DISTRIBUTION STATEMENT A
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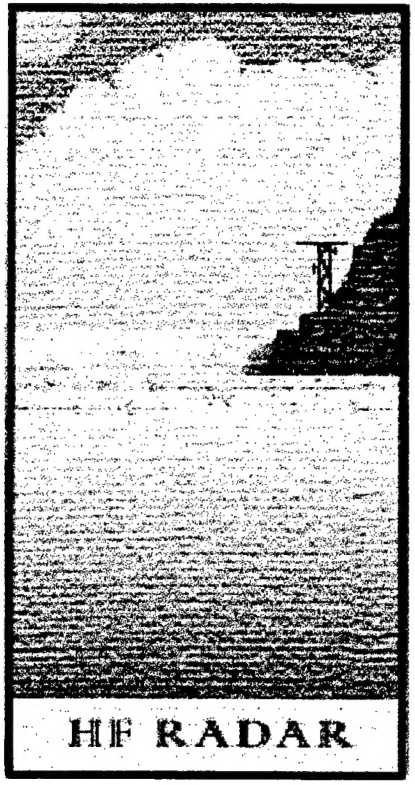
Distribution Unlimited



19971010 032

Volume II

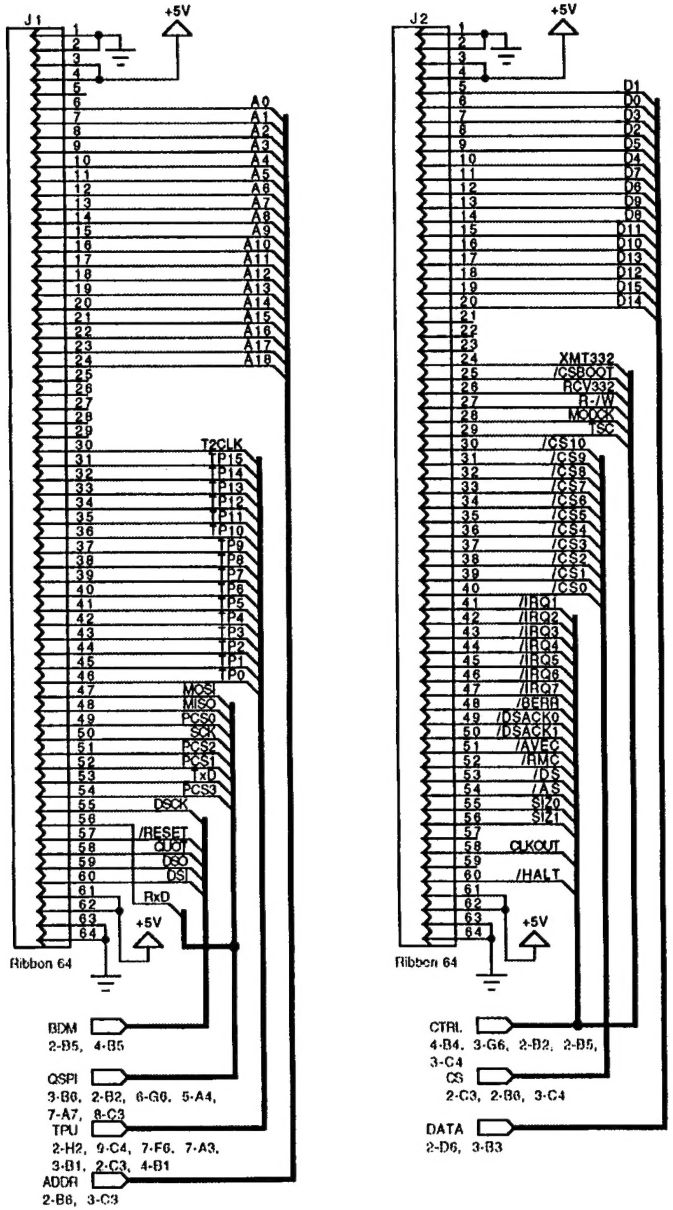
HF RADAR FINAL REPORT
University of Michigan Projects 032882 & 032887

ONR GRANTS: N00014-95-1-0367 & N00014-95-1-0249

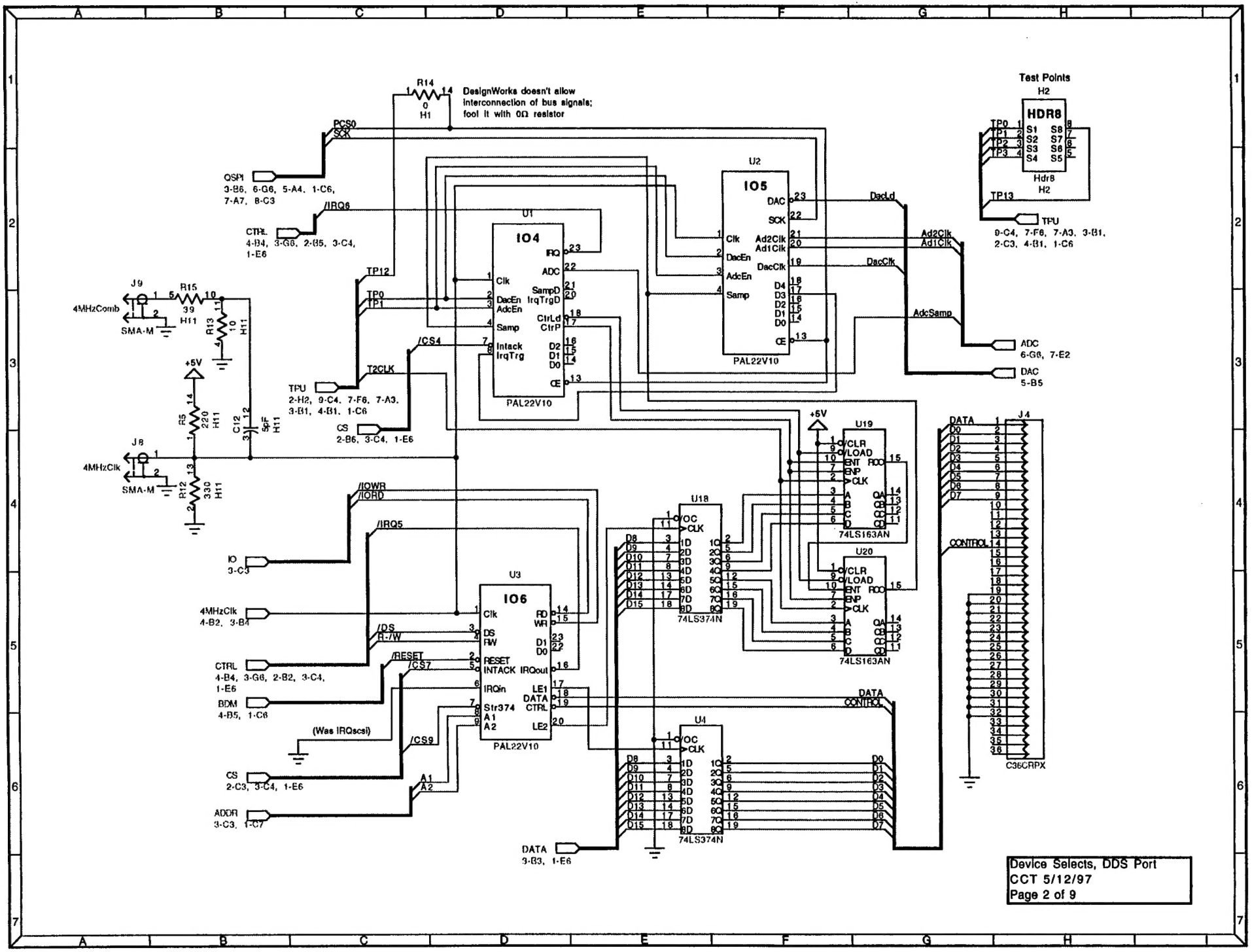
DTIC QUALITY INSPECTED 3

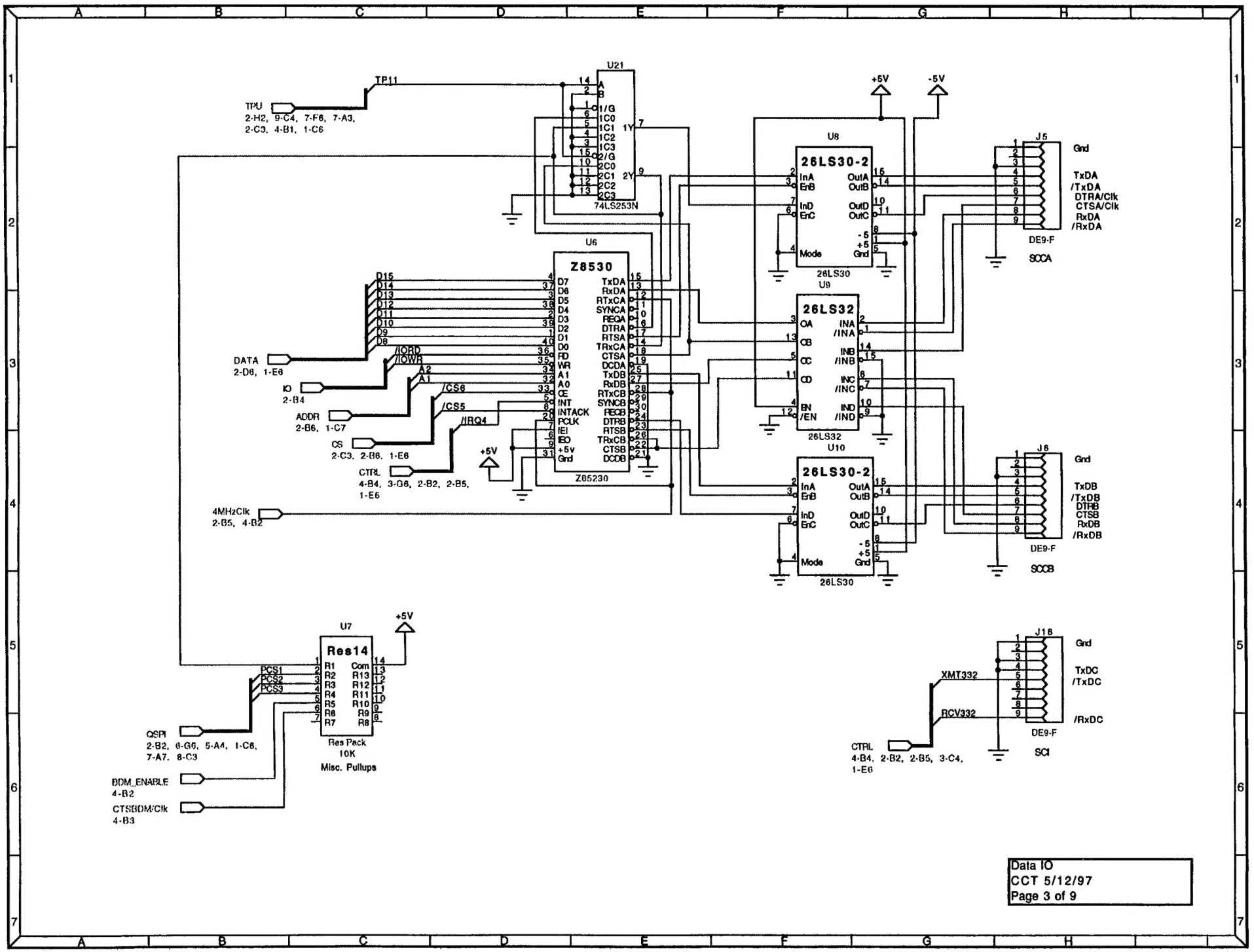
SYSTEM DOCUMENTATION (STANFORD)

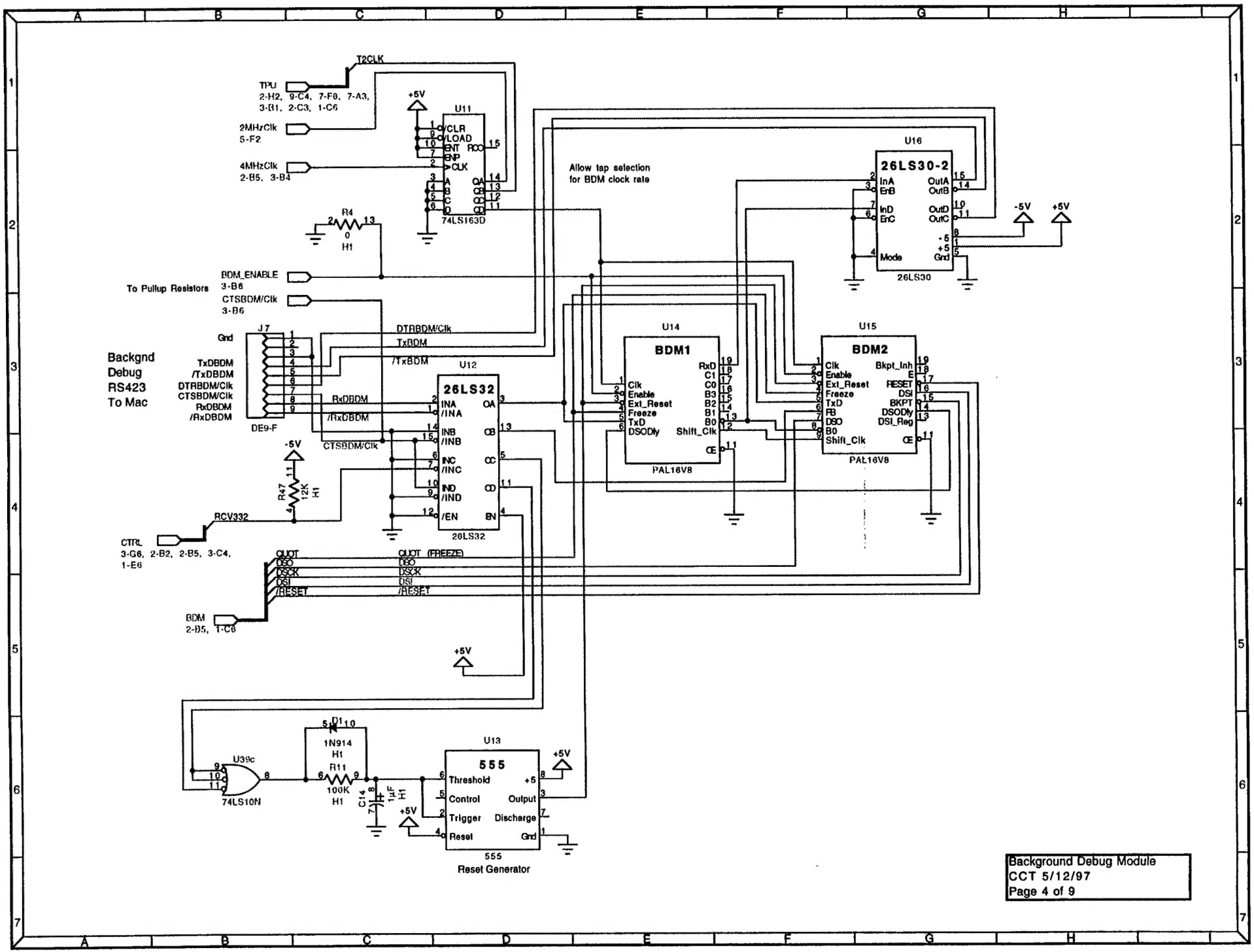
DTIC QUALITY INSPECTED 3

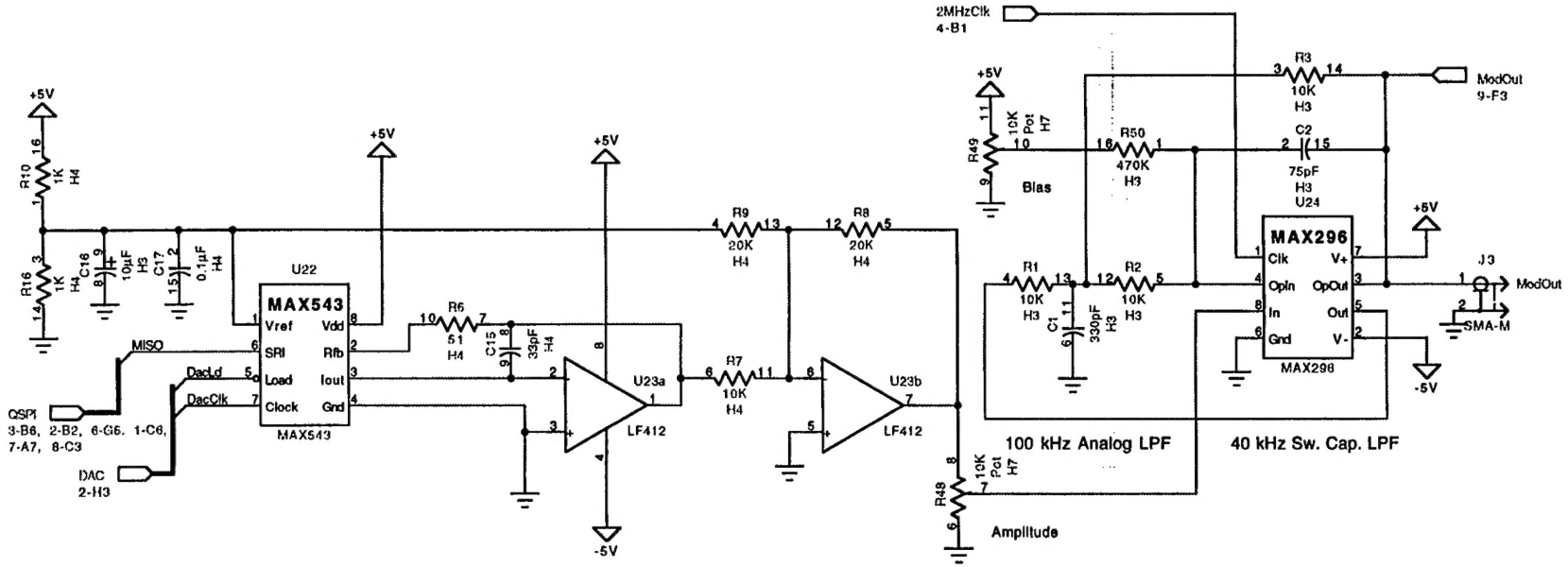


68332 Interface
CCT 5/12/97
Page 1 of 9


R14
0
H1
DesignWorks doesn't allow interconnection of bus signals; foot it with 0Ω resistor
PCS0
SCK
QSPI
3-B6, 6-G6, 5-A4, 1-C6, 7-A7, 8-C3
/IRQ6
CTRL
4-B4, 3-G6, 2-B5, 3-C4, 1-E6
U1
104
IRQ
ADC
Clk
SampD
DacEn
IrqTrgD
AdcEn
CtrLd
Samp
CtrP
Intack
IrqTrg
D2
D1
D0
CE
PAL22V10
U2
105
DAC
SCK
Clk
Ad2Clk
Ad1Clk
DacEn
DacClk
AdcEn
Samp
D4
D3
D2
D1
D0
CE
PAL22V10
DacLd
Ad2Clk
Ad1Clk
DacClk
AdcSamp
ADC
6-G6, 7-E2
DAC
5-B5
Test Points
H2
HDR8
TP0
TP1
TP2
TP3
S1
S2
S3
S4
S8
S7
S6
S5
Hdr8
H2
TP13
TPU
9-C4, 7-F6, 7-A3, 3-B1, 2-C3, 4-B1, 1-C6
J9
4MHzComb
SMA-M
R15
39
H11
R13
10
H11
+5V
R5
220
H11
C12
5pF
H11
J8
4MHzClk
SMA-M
R12
330
H11
TP12
TP0
TP1
TPU
2-H2, 9-C4, 7-F6, 7-A3, 3-B1, 4-B1, 1-C6
T2CLK
/CS4
CS
2-B6, 3-C4, 1-E6
/IOWR
/IORD
/IRQ5
IO
3-C3
4MHzClk
4-B2, 3-B4
/DS
R-/W
CTRL
4-B4, 3-G6, 2-B2, 3-C4, 1-E6
/RESET
/CS7
BDM
4-B5, 1-C6
(Was IRQscsi)
/CS9
CS
2-C3, 3-C4, 1-E6
ADDR
3-C3, 1-C7
A1
A2
U3
106
Clk
RD
WR
DS
R/W
D1
D0
RESET
INTACK
IRQout
IRQin
LE1
DATA
Str374
CTRL
A1
A2
LE2
PAL22V10
DATA
3-B3, 1-E6
U4
/OC
CLK
D8
D9
D10
D11
D12
D13
D14
D15
1D
2D
3D
4D
5D
6D
7D
8D
74LS374N
U18
74LS374N
U19
/CLR
/LOAD
ENT
ENP
CLK
RCO
A
B
C
D
QA
QB
QC
QD
74LS163AN
U20
74LS163AN
+5V
DATA
CONTROL
J4
D0
D1
D2
D3
D4
D5
D6
D7
CONTROL
C36CRPX
Device Selects, DDS Port
CCT 5/12/97
Page 2 of 9


TP11
TPU
2-H2, 9-C4, 7-F6, 7-A3,
2-C3, 4-B1, 1-C6
U21
74LS253N
U6
Z8530
Z85230
U8
26LS30-2
26LS30
U9
26LS32
U10
+5V
-5V
J5
DE9-F
SCCA
J6
SCCB
TxDA
/TxDA
DTRA/Clk
CTSA/Clk
RxDA
/RxDA
TxDB
/TxDB
DTRB
CTSB
RxDB
/RxDB
Gnd
DATA
2-D6, 1-E6
IO
2-B4
ADDR
2-B6, 1-C7
CS
2-C3, 2-B6, 1-E6
CTRL
4-B4, 3-G6, 2-B2, 2-B5,
1-E6
/IORD
/IOWR
A2
A1
/CS6
/CS5
/IRQ4
4MHzClk
2-B5, 4-B2
U7
Res14
Res Pack
10K
Misc. Pullups
QSPI
2-B2, 6-G6, 5-A4, 1-C6,
7-A7, 8-C3
BDM_ENABLE
4-B2
CTSBDM/Clk
4-B3
J16
XMT332
RCV332
/RxDC
SCI
CTRL
4-B4, 2-B2, 2-B5, 3-C4,
1-E6
Data IO
CCT 5/12/97
Page 3 of 9


T2CLK
TPU
2-H2, 9-C4, 7-F8, 7-A3,
3-B1, 2-C3, 1-C6
2MHzClk
5-F2
4MHzClk
2-B5, 3-B4
+5V
U11
/CLR
/LOAD
ENT
ENP
CLK
RCO
QA
QB
QC
QD
A
B
C
D
74LS163D
R4
0
H1
BDM_ENABLE
3-B6
To Pullup Resistors
CTSBDM/Clk
3-B6
Gnd
J7
TxDBDM
/TxDBDM
DTRBDM/Clk
CTSBDM/Clk
RxDBDM
/RxDBDM
DE9-F
Backgnd
Debug
RS423
To Mac
DTRBDM/Clk
TxBDM
/TxBDM
RxDBDM
/RxDBDM
CTSBDM/Clk
U12
26LS32
INA
/INA
INB
/INB
INC
/INC
IND
/IND
/EN
OA
OB
OC
OD
EN
26LS32
-5V
R47
12K
H1
RCV332
CTRL
3-G6, 2-B2, 2-B5, 3-C4,
1-E6
QUOT
DSO
DSCK
DSI
/RESET
QUOT (FREEZE)
DSO
DSCK
DSI
/RESET
BDM
2-B5, 1-C6
Allow tap selection
for BDM clock rate
U16
26LS30-2
InA
InB
InD
InC
Mode
OutA
OutB
OutD
OutC
-5
+5
Gnd
26LS30
-5V
+5V
U14
BDM1
Clk
Enable
Ext_Reset
Freeze
TxD
DSODly
RxD
C1
C0
B3
B2
B1
B0
Shift_Clk
OE
PAL16V8
U15
BDM2
Clk
Enable
Ext_Reset
Freeze
TxD
FB
DSO
B0
Shift_Clk
Bkpt_Inh
E
RESET
DSI
BKPT
DSODly
DSI_Reg
OE
PAL16V8
U39c
74LS10N
D1
1N914
H1
R11
100K
H1
C14
1µF
H1
U13
555
Threshold
Control
Trigger
Reset
+5
Output
Discharge
Gnd
555
Reset Generator
Background Debug Module
CCT 5/12/97
Page 4 of 9



DAC Module (Modulator)
CCT 5/12/97
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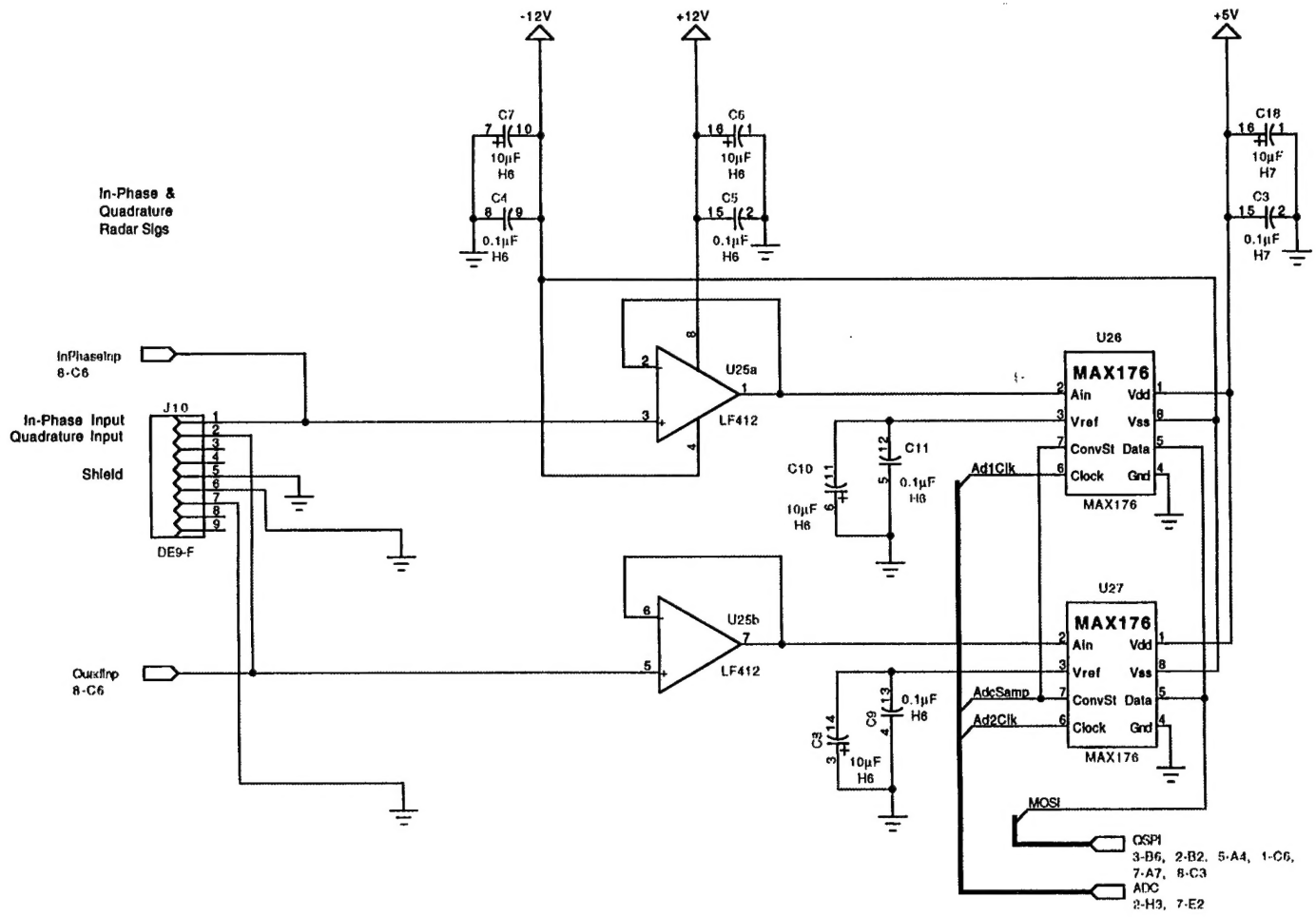

ADC Module
CCT 5/12/97
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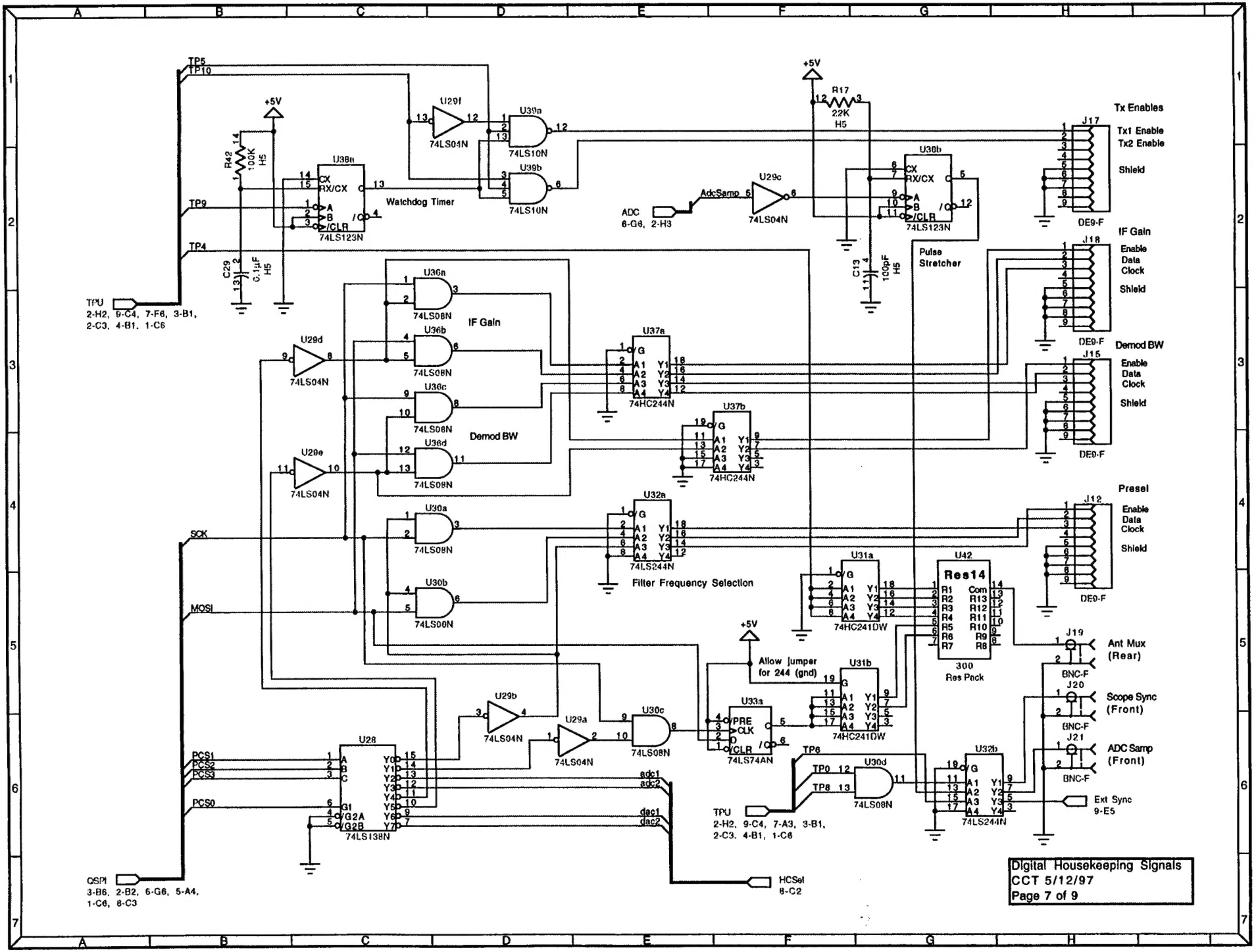
TP5
TP10
+5V
U29f
74LS04N
U39a
74LS10N
U39b
74LS10N
R42
100K
H5
U38a
74LS123N
Watchdog Timer
TP9
TP4
C29
0.1µF
H5
TPU
2-H2, 9-C4, 7-F6, 3-B1,
2-C3, 4-B1, 1-C6
ADC
6-G6, 2-H3
AdcSamp
U29c
74LS04N
R17
22K
H5
U38b
74LS123N
C13
100pF
H5
Pulse
Stretcher
Tx Enables
J17
Tx1 Enable
Tx2 Enable
Shield
DE9-F
IF Gain
J18
Enable
Data
Clock
Shield
DE9-F
Demod BW
J15
Enable
Data
Clock
Shield
DE9-F
Presel
J12
Enable
Data
Clock
Shield
DE9-F
U36a
74LS08N
IF Gain
U36b
74LS08N
U36c
74LS08N
Demod BW
U36d
74LS08N
U29d
74LS04N
U29e
74LS04N
U37a
74HC244N
U37b
74HC244N
U32a
74LS244N
Filter Frequency Selection
U30a
74LS08N
U30b
74LS08N
SCK
MOSI
U31a
74HC241DW
U42
Res14
300
Res Pack
U31b
74HC241DW
+5V
Allow jumper
for 244 (gnd)
U33a
74LS74AN
U29b
74LS04N
U29a
74LS04N
U30c
74LS08N
U28
74LS138N
PCS1
PCS2
PCS3
PCS0
adc1
adc2
dac1
dac2
TP6
TP0
TP8
U30d
74LS08N
TPU
2-H2, 9-C4, 7-A3, 3-B1,
2-C3, 4-B1, 1-C6
U32b
74LS244N
J19
Ant Mux
(Rear)
BNC-F
J20
Scope Sync
(Front)
BNC-F
J21
ADC Samp
(Front)
BNC-F
Ext Sync
9-E5
QSPI
3-B6, 2-B2, 6-G6, 5-A4,
1-C6, 8-C3
HCSel
8-C2
Digital Housekeeping Signals
CCT 5/12/97
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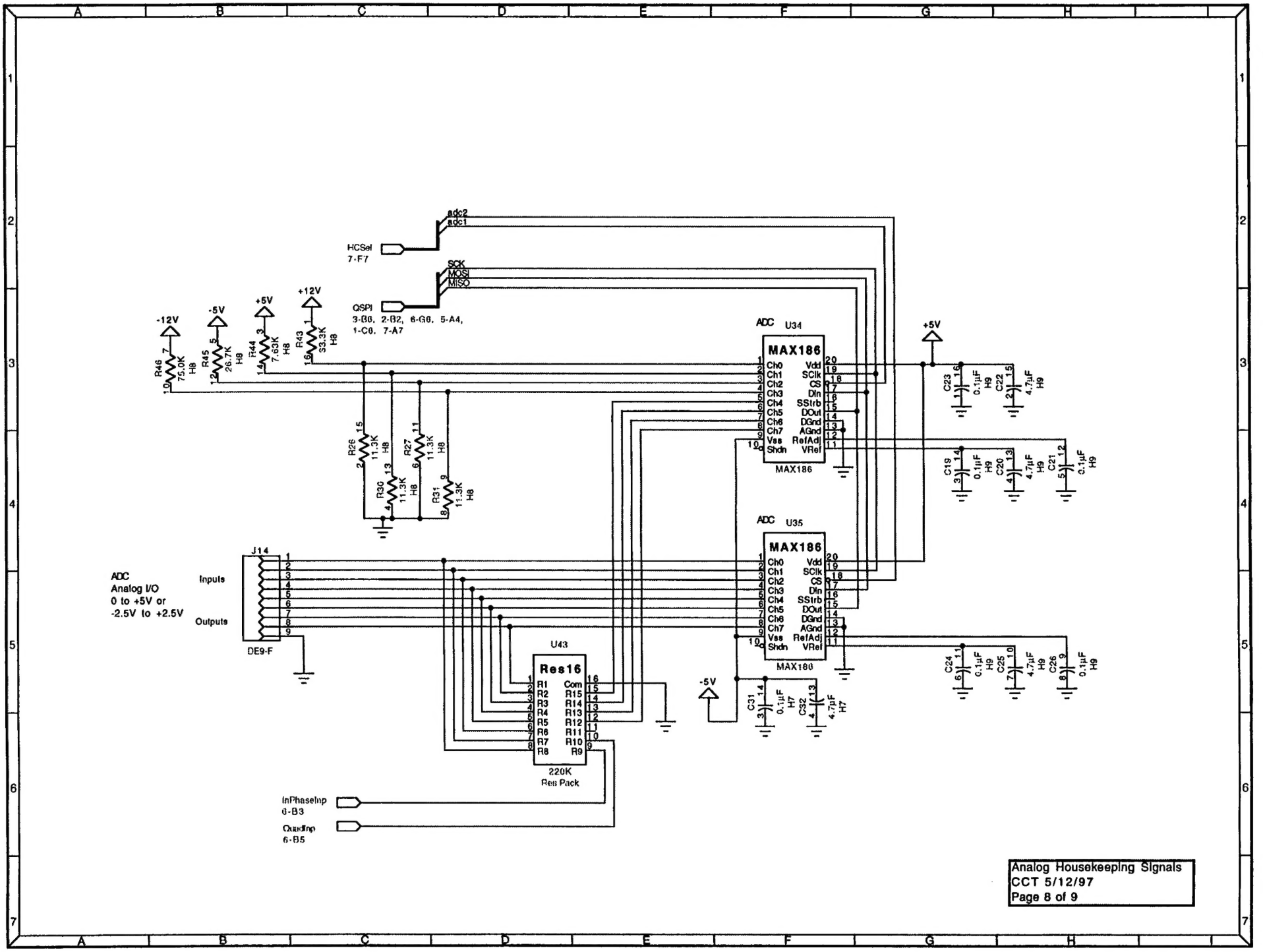

Analog Housekeeping Signals
CCT 5/12/97
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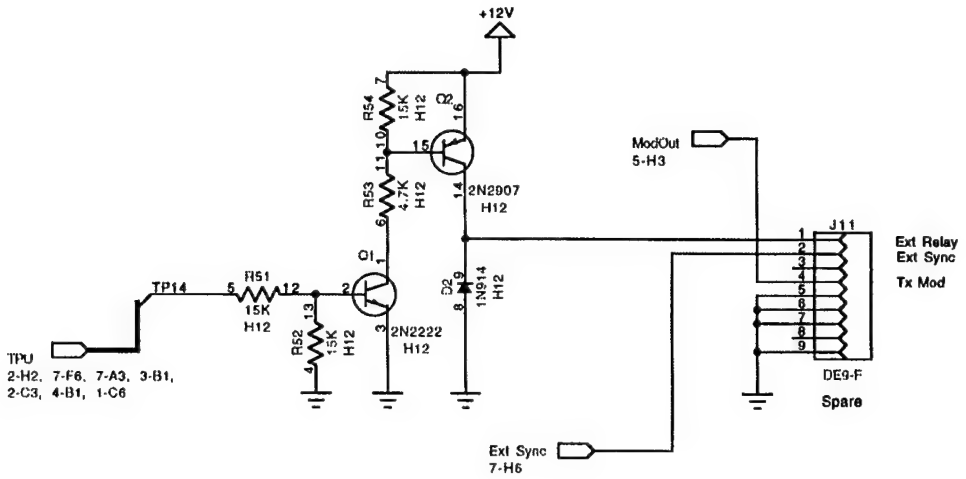

External Sync
CCT 5/12/97
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GROUP A
GROUP B
GROUP C
VCC
GND
J1
J2
U14 16V8
U15 16V8
U1 22V10
U2 22V10
U3 22V10
U20 74LS163
U19 74LS163
U11 74LS163
U38 74LS123
U29 74LS04
U36 74LS08
U30 74LS08
U33 74LS74
U39 74LS10
U37 74HC244
U31 74HC241
U4 74LS374
U18 74LS374
U21 74LS253
U28 74LS138
U12 26LS32
U16 26LS30
U9 26LS32
U8 26LS30
U10 26LS30
U32 74HC244
U22 543
U23 1458
U24 296
U25 1458
U26 176
U27 176
U34 MAX186
U35 MAX186
U43 Res
H 1 Comp
H 2 TP
H 3 Comp
H 4 Comp
H 5 Comp-14
H 6 Comp
H 7 Comp-14
H 8 Comp
H 9 Comp
H 10 Coax
H 11 4MHz
H 12 Comp
U6 Z85230
U13 555
U42 Res-14
U7 Res-14
J1 P1 DIP16
J1 P2 DIP16
J1 P3 DIP16
J1 P4 DIP16
J2 P5 DIP16
J2 P6 DIP16
J2 P7 DIP16
J2 P8 DIP16
STANFORD UNIVERSITY
68332 Field Experiment I/O
N/000149510249
68332 Field Exp Layout
1 OF 1

NET NAME	PINS							
/CS4	P7-2	U1-7						
/CS5	P7-15	U6-8						
/CS6	P7-1	U6-33						
/CS7	P7-16	U3-5						
/CS9	P6-9	U3-7						
/DS	P8-14	U3-3						
/IORD	U3-14	U6-36						
/IOWR	U3-15	U6-35						
/IRQ4	P7-6	U6-5						
/IRQ5	P7-10	U3-16						
/IRQ6	P7-7	U1-23						
/RESET	P4-12	U3-2	U15-17					

NET NAME	PINS							
/RxDBDM	BJ2-21	U12-1						
/TxBDM	BJ2-1	U16-14						
2MHzClk	U11-14	U24-1						
4MHzClk	H11-3	H11-7	H11-1	H11-13	U1-1	U2-1		
	U3-1	U6-12	U6-20	U6-28	U11-2			
4MHzComb	H11-6	H11-5						
A1	P1-13	U3-8	U6-32					
A2	P1-4	U3-9	U6-34					
Ad1Clk	U2-20	U26-6						
Ad2Clk	U2-21	U27-6						
AdcSamp	U1-22	U26-7	U27-7	U29-5				
BDM_ENABLE	H1-13	U7-5	U14-2	U15-2				
CONTROL	AJ1-27	U3-19						

NET NAME	PINS							
CTSBDM/Clk	BJ2-23	U7-6	U12-10	U12-15				
D0	AJ1-39	U4-2						
D1	AJ1-38	U4-5						
D2	AJ1-37	U4-6						
D3	AJ1-36	U4-9						
D4	AJ1-35	U4-12						
D5	AJ1-34	U4-15						
D6	AJ1-33	U4-16						
D7	AJ1-32	U4-19						
D8	P5-7	U4-3	U6-40	U18-3				
D9	P5-10	U4-4	U6-1	U18-4				
D10	P5-8	U4-7	U6-39	U18-7				
D11	P5-9	U4-8	U6-2	U18-8				
D12	P6-1	U4-13	U6-38	U18-13				

NET NAME	PINS							
D13	P6-16	U4-14	U6-3	U18-14				
D14	P6-2	U4-17	U6-37	U18-17				
D15	P6-15	U4-18	U6-4	U18-18				
DATA	AJ1-40	U3-18						
DSCK	P4-13	U15-15						
DSI	P4-6	U15-16						
DSO	P4-11	U15-7						
DTRBDM/Clk	BJ2-24	U16-11						
DacClk	U2-19	U22-7						
DacLd	U2-23	U22-5						
Ext_Sync	BJ1-27	U32-5						
Ground	H3-6	H7-2	H6-8	H6-2	H6-1	H6-7	H6-3	
	H6-4	H6-6	H6-5	H5-11	H1-7	H3-8	H4-15	
	H7-1	H9-3	H9-4	H9-5	H9-2	H9-1	H9-6	
	H9-7	H9-8	H5-13	H7-3	H7-4	H12-8	P1-16	
	P1-1	P4-9	P4-8	P5-16	P5-1	P8-9	P8-8	

NET NAME	PINS							
	H10-1	AJ1-20	AJ1-19	AJ1-18	AJ1-17			
	AJ1-16	AJ1-15						
	AJ1-14	AJ1-13	AJ1-12	AJ1-11	AJ1-10	AJ1-9		
	AJ1-8	AJ1-7	BJ2-11	BJ2-7	BJ2-3	H11-8	H11-9	
	CJ1-15	CJ1-14	BJ1-8	BJ1-7	BJ1-5	BJ1-12	BJ1-11	
	BJ1-10	CJ1-17	BJ1-16	BJ1-15	BJ1-14			
	BJ2-15	BJ2-14	BJ2-20	BJ2-19	BJ1-20			
	BJ1-19	BJ1-18	BJ1-2	AJ1-1	AJ1-2	H12-3		
	H1-2	H11-2	H11-4	H4-14	H8-2	H8-6	H8-4	H8-8
	H7-6	H7-9	H12-4	U1-12	U2-12	U3-12	U4-1	
	U4-10	U6-19	U6-21	U6-31	U8-4	U8-5	U8-6	
	U9-8	U9-9	U9-12	U9-15	U10-4	U10-5	U10-6	
	U11-3	U11-4	U11-5	U11-6	U11-8	U12-6		
	U12-8	U12-9	U12-12	U12-14	U13-1			
	U14-10	U14-11	U15-10	U15-11	U16-3	U16-4		
	U16-5	U16-6	U18-1	U18-10	U19-8	U20-8		
	U21-1	U21-2	U21-3	U21-4	U21-8			
	U21-11	U21-12	U21-13	U22-4	U23-3	U23-5		
	U24-6	U26-4	U27-4	U28-4	U28-5	U28-8		
	U29-7	U30-7	U31-1	U31-10	U32-1	U32-8		
	U32-10	U32-17	U32-19	U33-7	U34-13			
	U34-14	U35-13	U35-14	U36-7	U37-1			
	U37-10	U37-15	U37-17	U37-19	U38-6	U38-8		
	U38-14	U39-7	U43-16					
InPhaseInp	CJ1-35	U25-3	U43-9					

NET NAME	PINS							
MISO	P3-8	U22-6	U34-15	U35-15				
MOSI	P3-9	U26-5	U27-5	U30-5	U33-2			
		U34-17	U35-17	U36-4	U36-12			
Minus5V	H7-14	H7-13	H8-5	H1-11	U8-8	U10-8		
		U16-8	U23-4	U24-2	U34-9	U35-9		
Minus12V	H6-9	H6-10	H8-7	U25-4	U26-8	U27-8		
ModOut	H3-15	H10-8	H3-14	U24-3	BJ1-25			
PCS0	P4-16	H1-14	U1-13	U2-13	U28-6			
PCS1	P4-2	U7-2	U28-1					
PCS2	P4-15	U7-3	U28-2					

NET NAME	PINS							
PCS3	P4-3	U7-4	U28-3					
Plus5V	H7-15	H7-16	H9-15	H9-16	H11-14			
	H4-16	H5-12	H5-14	H8-3	H7-11	U1-24		
	U2-24	U3-24	U4-20	U6-7	U6-9	U7-14		
	U8-1	U9-4	U9-16	U10-1	U11-1	U11-7		
	U11-9	U11-10	U11-16	U12-4	U12-16			
	U13-4	U13-8	U14-20	U15-20	U16-1			
	U18-20	U19-1	U19-16	U20-1	U20-16			
	U21-16	U22-8	U23-8	U24-7	U26-1			
	U27-1	U28-16	U29-14	U30-14	U31-19			
	U31-20	U32-20	U33-1	U33-4	U33-14			
	U34-20	U35-20	U36-14	U37-20	U38-2			
	U38-3	U38-10	U38-11	U38-16	U39-14			
Plus12V	H6-15	H6-16	H12-16	H8-1	H12-7	U25-8		
QUOT	P4-5	U14-4	U15-4					

NET NAME	PINS							
QuadInp	CJ1-34	U25-5	U43-10					
R-/W	P6-11	U3-4						
RCV332	P6-5	BJ2-33	H1-4	U12-7				
RxDBDM	BJ2-22	U12-2						
SCK	P4-1	U2-22	U30-2	U30-9	U34-19	U35-19		
		U36-1	U36-9					
SIG809	U6-22	U6-26	U9-11					
SIG810	U6-23	U10-3						
SIG811	U6-24	U10-7						
SIG815	U6-27	U9-5						
SIG816	U6-25	U10-2						
SIG820	U6-17	U8-3						
SIG825	U6-13	U9-3						
SIG826	U6-15	U8-2						

NET NAME	PINS							
SIG882	BJ2-32	U8-11						
SIG884	BJ2-10	U8-15						
SIG886	BJ2-27	U9-10						
SIG887	BJ2-25	U9-7						
SIG888	BJ2-26	U9-6						
SIG890	BJ2-31	U9-14						
SIG891	BJ2-29	U9-1						
SIG892	BJ2-30	U9-2						
SIG893	BJ2-28	U10-11						
SIG895	BJ2-5	U10-14						
SIG896	BJ2-6	U10-15						
SIG898	BJ2-9	U8-14						
SIG1302	U25-1	U25-2	U26-2					
SIG1318	H6-11	H6-12	U26-3					

NET NAME	PINS							
SIG1453	U12-3	U14-5	U15-5					
SIG1454	U13-3	U14-3	U15-3					
SIG1456	U14-12	U15-9						
SIG1457	U14-6	U15-14						
SIG1458	U12-11	U39-11						
SIG1460	U14-13	U15-8	U16-7					
SIG1461	U14-19	U16-2						
SIG1470	U11-11	U14-1	U15-1					
SIG1603	U25-6	U25-7	U27-2					
SIG1610	H6-14	H6-13	U27-3					
SIG1662	H4-10	U22-2						
SIG1665	H4-8	H4-7	H4-6	U23-1				
SIG1667	H4-9	U22-3	U23-2					
SIG1676	H4-11	H4-12	H4-13	U23-6				

NET NAME	PINS							
SIG2078	U3-20	U18-11						
SIG2100	U1-8	U2-17						
SIG2110	U1-17	U19-7	U19-10	U20-7				
SIG2111	U1-18	U19-9	U20-9					
SIG2167	U3-17	U4-11						
SIG2183	U18-2	U19-3						
SIG2184	U18-5	U19-4						
SIG2185	U18-6	U19-5						
SIG2186	U18-9	U19-6						
SIG2187	U18-12	U20-3						
SIG2188	U18-15	U20-4						
SIG2189	U18-16	U20-5						
SIG2190	U18-19	U20-6						
SIG2212	U19-15	U20-10						

NET NAME	PINS							
SIG2226	U1-4	U2-4	U20-15					
SIG2253	U8-7	U21-7						
SIG2256	U6-18	U9-13	U21-10					
SIG2259	U6-16	U21-6						
SIG2264	U6-14	U7-1	U21-5	U21-9				
SIG2276	H3-4	U24-5						
SIG2294	H7-7	U24-8						
SIG2297	H3-11	H3-13	H3-12	H3-3				
SIG2306	H3-9	H4-2	H4-4	H4-1	H4-3	U22-1		
SIG2567	U30-3	U32-2						
SIG2568	U28-10	U29-11						
SIG2571	U30-6	U32-4						
SIG2572	U28-14	U29-1						
SIG2573	U29-2	U30-10						

NET NAME	PINS							
SIG2574	U28-15	U29-3						
SIG2575	U29-4	U30-1	U30-4	U32-6				
SIG2578	BJ1-31	U32-16						
SIG2580	U31-18	U42-1						
SIG2581	U31-16	U42-2						
SIG2582	U31-14	U42-3						
SIG2583	U31-12	U42-4						
SIG2585	U31-7	U42-6						
SIG2610	H9-14	H9-13	U34-11					
SIG2611	H9-12	U34-12						
SIG2612	H8-15	H8-16	U34-1					
SIG2613	H8-11	H8-12	U34-3					
SIG2616	H8-13	H8-14	U34-2					
SIG2617	H8-9	H8-10	U34-4					

NET NAME	PINS							
SIG2622	H9-11	H9-10	U35-11					
SIG2623	H9-9	U35-12						
SIG2644	U31-11	U31-13	U31-15	U31-17	U33-5			
SIG2646	U30-8	U33-3						
SIG2841	U36-11	U37-8						
SIG2843	U29-8	U36-2	U36-5	U37-11				
SIG2844	U36-3	U37-2						
SIG2847	U36-6	U37-4						
SIG2850	U36-8	U37-6						
SIG2856	BJ1-35	U37-12						
SIG2864	U28-11	U29-9						
SIG2880	U29-10	U36-10	U36-13	U37-13				
SIG2942	H5-2	H5-1	U38-15					
SIG2946	U38-13	U39-5	U39-13					

NET NAME	PINS	
SIG2961	BJ2-40	U39-12
SIG2967	U29-12	U39-1
SIG2975	BJ2-39	U39-6
SIG2995	BJ1-38	U37-18
SIG2996	BJ1-40	U37-9
SIG3006	BJ1-39	U37-16
SIG3008	BJ1-34	U37-14
SIG3012	BJ1-36	U37-7
SIG3023	BJ1-30	U32-18
SIG3024	BJ1-32	U32-14
SIG3025	U32-13	U38-5
SIG3028	AJ1-21	U32-9
SIG3029	AJ1-22	U32-7
SIG3049	U30-11	U32-11

NET NAME	PINS							
SIG3167	CJ1-18	U35-8	U43-1					
SIG3168	U12-5	U39-9	U39-10					
SIG3173	U12-13	U15-6						
SIG3185	H1-8	H1-10	H1-9	U13-2	U13-6			
SIG3186	H1-5	H1-6	U39-8					
SIG3207	H4-5	H7-8	U23-7					
SIG3213	H7-10	H3-16						
SIG3215	H3-2	H3-5	H3-1	U24-4				
SIG3220	H12-1	H12-6						
SIG3223	H12-9	BJ1-28	H12-14					
SIG3226	H12-2	H12-12	H12-13					
SIG3228	H12-15	H12-11	H12-10					
SIG3284	CJ1-40	U35-1	U43-8					
SIG3285	CJ1-39	U35-2	U43-7					

NET NAME	PINS							
SIG3286	CJ1-38	U35-3	U43-6					
SIG3287	CJ1-37	U35-4	U43-5					
SIG3288	CJ1-36	U35-5	U43-4					
SIG3289	CJ1-20	U35-6	U43-3					
SIG3300	U34-8	U43-12						
SIG3301	U34-7	U43-13						
SIG3302	U34-6	U43-14						
SIG3303	U34-5	U43-15						
SIG3314	U31-9	U42-5						
SIG3325	BJ1-22	U42-14						
SIG3372	CJ1-19	U35-7	U43-2					
SIG3392	H11-12	H11-11	H11-10					
SIG3425	H5-4	H5-3	U38-7					
SIG3439	U29-6	U38-9						

NET NAME	PINS							
T2CLK	P2-7	U11-13	U19-2	U20-2				
TP0	H2-1	P3-7	U1-2	U2-2	U30-12			
TP1	H2-2	P3-10	U1-3	U2-3				
TP2	H2-3	P3-6						
TP3	H2-4	P3-11						
TP4	P3-5	U31-2	U31-4	U31-6	U31-8			
TP5	P3-12	U39-2	U39-4					
TP6	P3-4	U32-15						
TP8	P3-3	U30-13						
TP9	P3-14	U38-1						
TP10	P3-2	U29-13	U39-3					
TP11	P3-15	U21-14	U21-15					
TP12	P3-1	H1-1						
TP13	H2-8	P3-16						

NET NAME	PINS	
TP14	P2-8	H12-5
TxBDM	BJ2-2	U16-15
XMT332	P6-4	BJ2-13
adc1	U28-13	U34-18
adc2	U28-12	U35-18

Vesta
SBC332 Family
Hardware Manual

vesta technology, inc.

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Technical support is available at no charge by fax to (303) 422-9800. Vesta will respond within twenty four (24) hours. Specifically excluded is any free support of efforts to program Vesta boards without Vesta firmware. Continuing engineering services are available on an hourly basis.

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Vesta will repair without charge any assembly or defects on units returned within the original warranty period. Testing and repair of user-damaged units, or units with expired warranties will be charged based on time and materials.

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7100 W. 44th Ave, Suite 101, Wheat Ridge, CO 80033 FAX: (303) 422-9800 **Voice: (303) 422-8088**

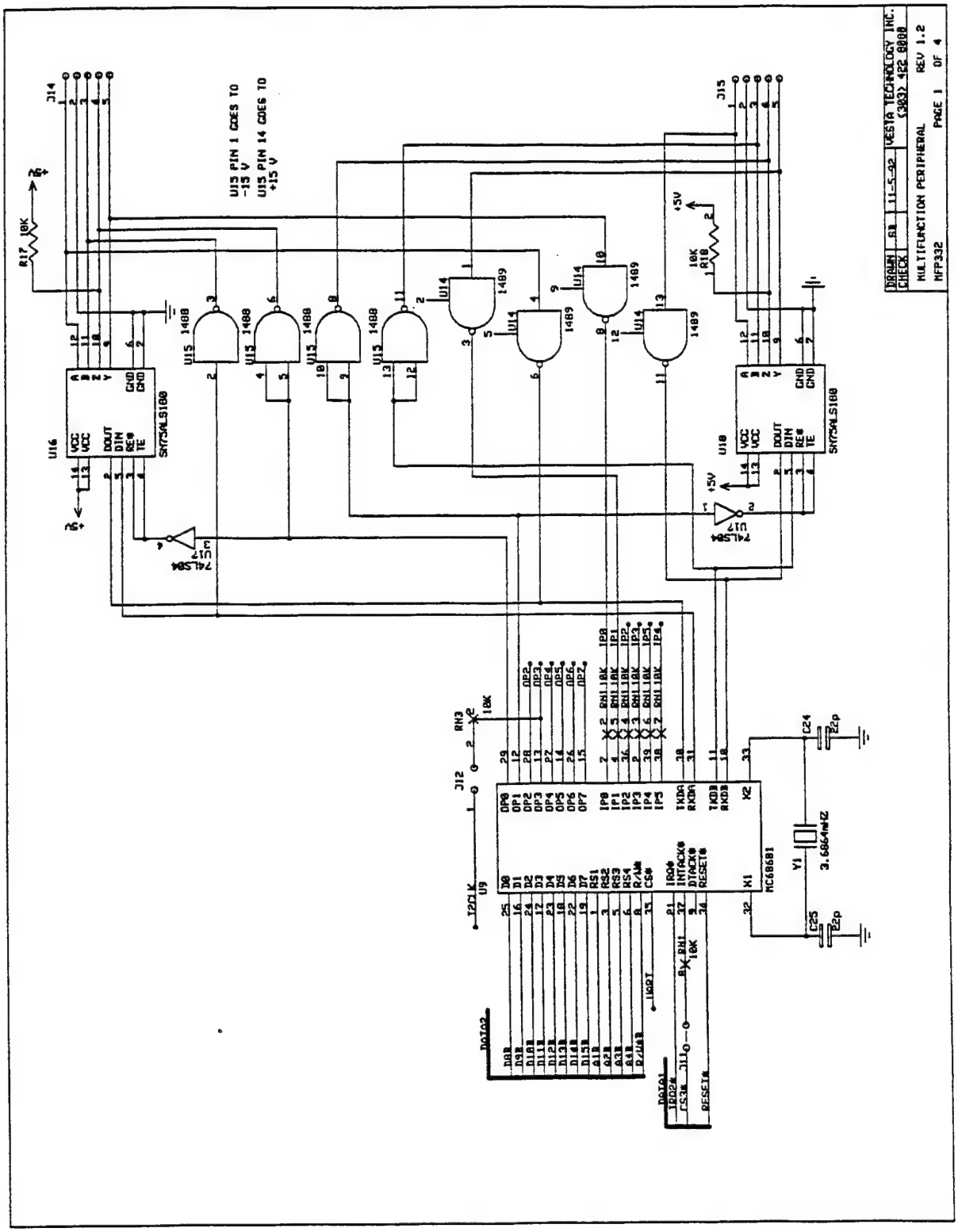
SBC332 Hardware Manual Rev. 1.3
Board Rev. 1.2 Errata

SBC332 Manual

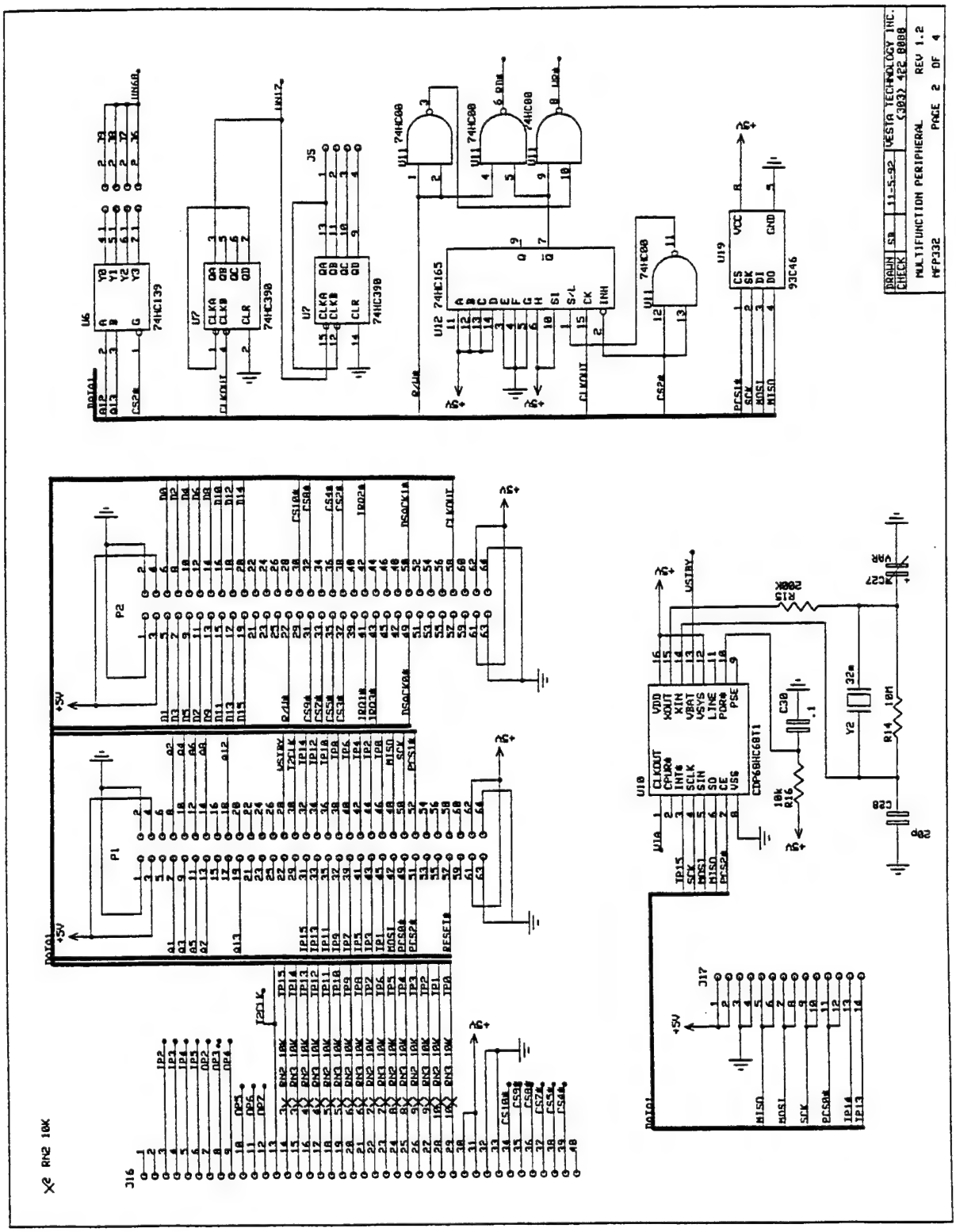
Board Revision Level 1.2: TPU channels 1 and 5 are configured for use with the serial transceiver, U7. Unlike board revision 1.3, there is no jumper J12 to release TPU channel 1 from the serial transceiver. To provide this feature and free channel 1 for other use, remove the serial transceiver U7, bend pin 10 outward, and re-install U7. To release channel 5 from the serial transceiver, remove jumper J10. With both channels 1 and 5 released, all the TPU channels are available without restriction for the user in any functionality as described in the Motorola TPU documentation.

September 20, 1993

SCHEMATIC, PART 1



SCHEMATIC, PART 2



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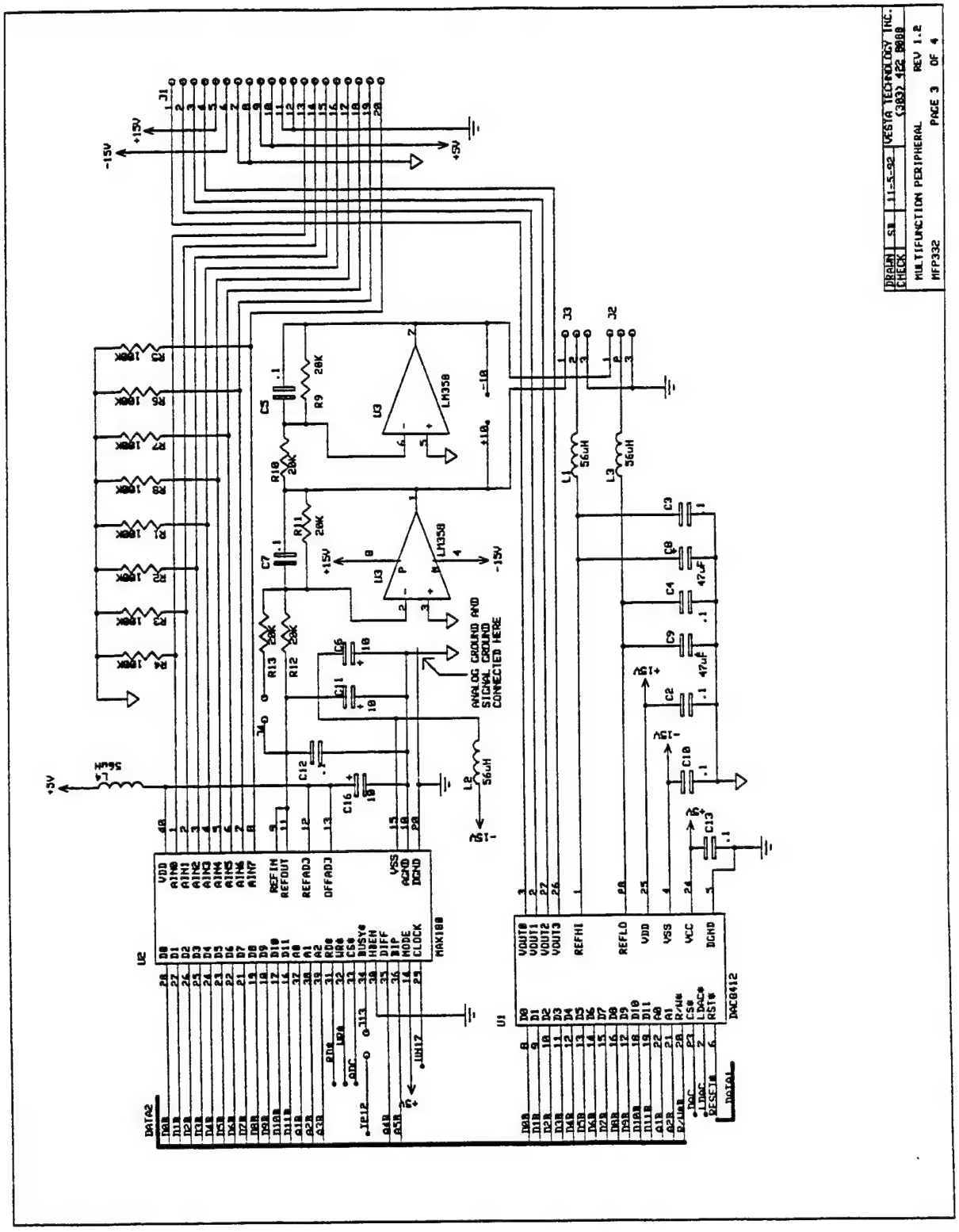
SCHEMATIC, PART 3



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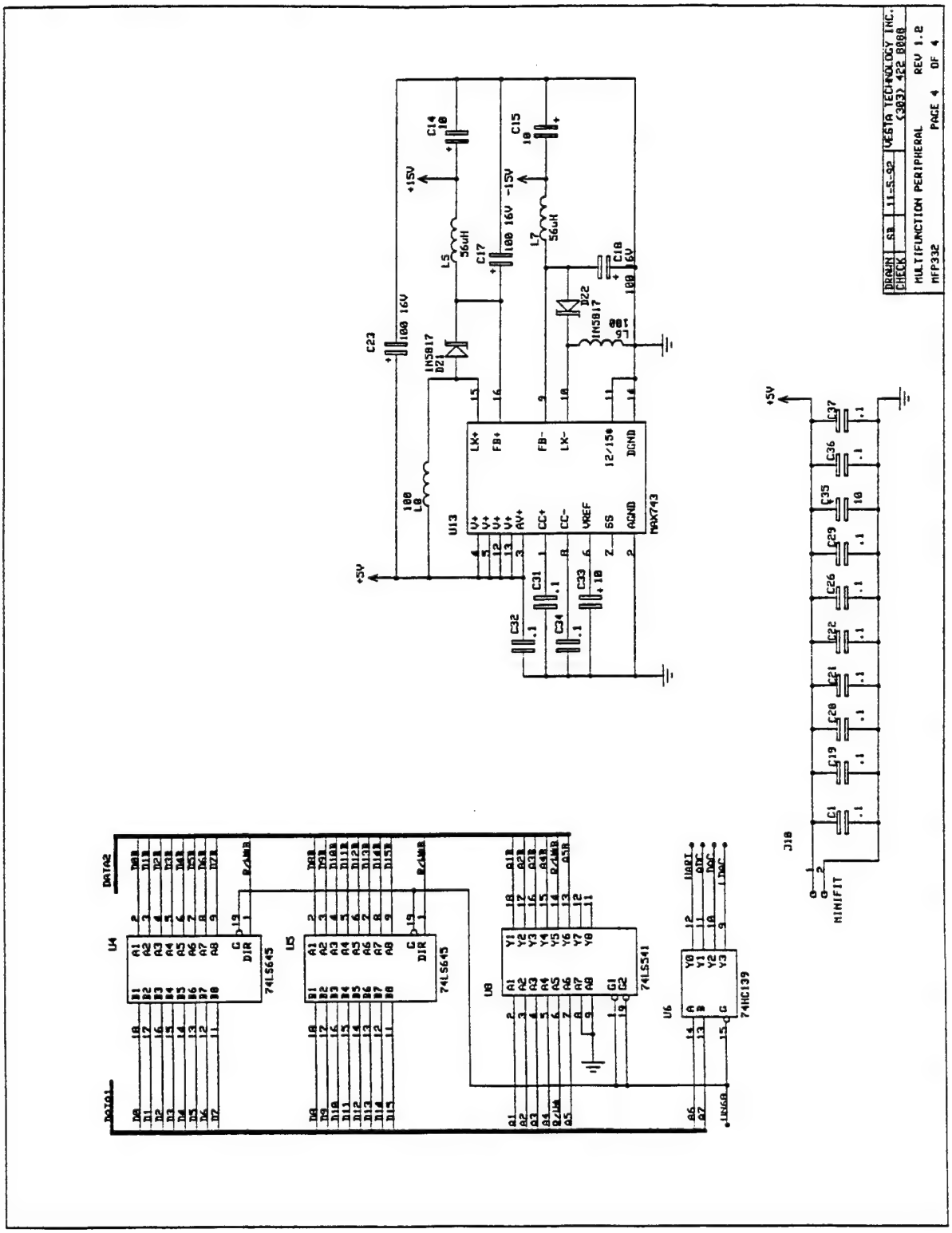
SCHEMATIC, PART 4



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The Use of 512k x 8 Pseudo-Static RAM Devices on the SBC332

It is possible to use 512kbyte pseudo-static RAM devices (psRAMs) on the SBC332 to obtain one megabyte of onboard RAM. There is a limitation which must be dealt with, however, and which has certain consequences. This limitation is that the psRAMs must be refreshed similarly to dynamic RAM devices. The refresh process requires reading each of the first 2kbytes of each device at least once every 32 milliseconds. The consequences are that the internal periodic interrupt timer (or some other interrupt source) is required to provide reliable invocation of the refresh function. Additionally, the overhead of refreshing the RAMs will cause the system to run slightly more slowly than when using fully-static RAMs.

Vesta Technology has written a short application program for VFSE-332 which will perform this refresh operation. It is found in the file PSEUDRAM.F on the utilities disk. In order to use psRAMs, this application must be placed into a pair of application EPROMs and configured as an autostart application. This means that you *must* have "normal" (static) RAM devices installed while you compile PSEUDRAM.F and save the new EPROM image. Once you have a new working set of EPROMs with this application autostarting, you can replace the static RAM devices with psRAMs.

If you are working in C or assembly, then you will have to incorporate the periodic refresh capability into your application code. The following assembly-language routine has been translated from VFSE-332 assembly format to Motorola assembly format. It has *not* been tested in this form.

```
PICR_value  equ         $07FF               ; level 7 interrupts, vector $FF
PITR_value  equ         $00F0               ; interrupt every 29.3 milliseconds
RAM_BASE    equ         $100000             ; start of RAM for VFSE-332

refresh:
            movem.l     d0-d1/a0, -(a7)     ; preserve D0, D1, and A0
            move.l      #1024, d1           ; number of 32-bit words to read
            move.l      RAM_BASE, a0
refresh_loop:
            move.l      (a0)+, d0           ; read 2 bytes from each device
            dbra        d1, refresh_loop
            movem.l     (a7)+, d0-d1/a0     ; restore the scratch registers
            rte
```

The address of the label "refresh" must be placed into the exception vector number $FF, and the periodic interrupt timer registers of the 68332 programmed with PICR_value and PITR_value. This code assumes that the 68332 is running at the full 16MHz clock speed. If you change the clock frequency of the 68332, you will have to change the PITR_value in order to keep interrupt occurring more often than once every 32 milliseconds.

Using this routine does require the use of the periodic interrupt timer capabilities of the 68332. If you need the periodic interrupt for other purposes, you will have to make the necessary modifications and compensations to allow the periodic interrupt timer to be shared by the functions, or you will have to provide some other manner of invoking the psRAM refresh.

vesta technology

SBC332

Revision 1. 3
April 16, 1993

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The SBC332

The SBC332 is closely related to the original Motorola "Business Card Computer" (BCC). The SBC332 is designed as a complete standalone engine for high performance OEM products. The SBC332 also supports the Vesta **WRITE IT • RUN IT • ROM IT** easy development process. Consequently, the SBC332 has several advantages over the BCC.

- DIP socketed, readily-available byte-wide memory devices
- choice of onboard memory device (RAM and/or ROM) size
- Socketed microprocessor for easy replacement
- Onboard reset generator
- Continuous-cycling external watchdog timer
- Power supply monitor
- Internal RAM backed for one hour
- BCC-compatible external bus pinout
- **Low cost, productive development environment.**

P1 and P2 Installation

The two 64 position Dual Row Headers, P1 and P2, have been supplied separately. You have the option of installing these connectors on either the solder or component side of the the SBC332 depending on your mechanical mounting requirements. Please specify your desired production configuration when you reorder.

Please note that these connectors must be installed on the component side for the pin numbers to be consistent with insulation displacement cables. P1 and P2 must be mounted on the component side for attachment to any other Vesta standard product.

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Quick Start

If you also purchased Vesta Forth Standard Edition for the SBC332 (VFSE-332), you can quickly bring up and test your Vesta SBC332. You need:

- A personal computer with text editor, communications program and serial port.
- An RS-232 cable from your computer to the SBC332 serial connector J5.
- A +5 Volt at 150 mA supply with cable to SBC332 power connector J1.
- Vesta Forth Standard Edition for the SBC332 (VFSE-332).

Turn on your personal computer. Start your favorite telecommunications program. Set the communications parameters for 8 data bits, no parity, 1 stop bit, 9600 baud.

Connect the serial cable to the SBC332 at **J5** (See diagram on page 7). Pin 1 of J5 is marked with an silkscreened asterisk on the SBC332.

Apply power to **J1**. Ground (-) and positive (+) are silkscreened on the board.

J1

Pin	Description
1	+5 VDC at 150 mA
2	Ground return

J1 POWER CONNECTOR

Once the serial cable is connected properly and power applied to the SBC332, your personal computer communications program will display the sign on message:

```
Vesta Forth Standard Edition - SBC332
Generated: yymmdd
```

on your screen. `yymmdd` are numbers which indicate the revision date (year, month, and date) of the VFSE-332 EPROMs. If you do not see this or a similar message, check the power connection, and try reversing the serial cable at J5. Reapply power.

Once you see the sign-on prompt, you may interactively compose and test Forth programs directly on the SBC332. Alternatively Using a text editor (or a word processor in text mode) in conjunction with your communications program on your personal computer, you can also download text files. An EPROM programmer capable of programming 27C256 or larger EPROMs is all that it takes to complete your embedded system development environment.

For more information on Vesta Forth Standard Edition, see the ***Vesta Forth Standard Edition Manual.***

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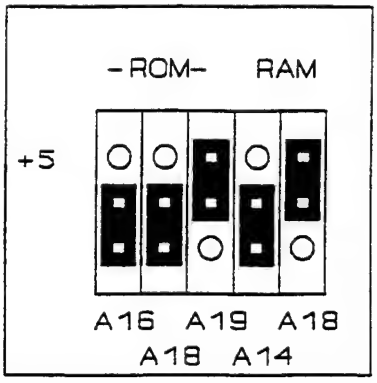
Memory

The SBC332 will accommodate either 32-pin or 28-pin byte-wide memory devices in 0.6" wide sockets. When 28-pin devices are inserted into the 32-position sockets, pins 1, 2, 31 and 32 of the socket should be empty.

Memory Selection

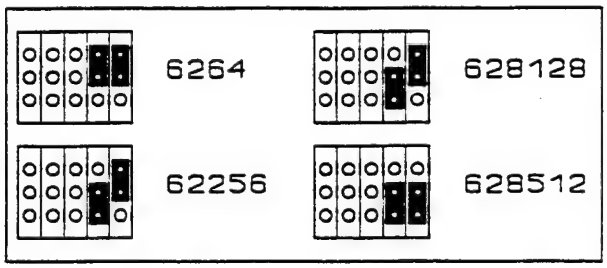
RAM and ROM devices of various capacities may be installed in the SBC332. In general, a few pins must be accomodated to switch between these sizes. Jumper block **J2** allows a variety of devices and is shown in Figure 1. The orientation of the diagram is such that the dual-row header P2 would to the right of the jumper block shown.



RAM

Sockets **U6** (RAM HI) and **U2** (RAM LO) contain 8k/32k/128k/512k static RAM integrated circuits in .6" wide DIP packages. The SBC332 requires two RAMs of equal capacity.

The figure at the right indicates Jumper **J2** positions for the various devices. The table below summarizes the pins and their functions that must be changed to change RAM size. "Pin 28" and "pin 30" refer to a 32 pin DIP integrated circuit. Once again, the orientation of the diagram is such that the dual-row header P2 would be to the right of the jumper block(s) shown.



Size	Type	Pin 28	Pin 30
8k	6264	+5	+5
32k	62256	A14	+5
128k	628128	A14	+5
512k	628512	A14	A18

SRAM SIZES, TYPES AND VARIANT PIN DESCRIPTIONS

Pins 28 of both RAMs are connected to the fourth jumper position. Pins 30 of both RAMs are connected to the fifth jumper position.

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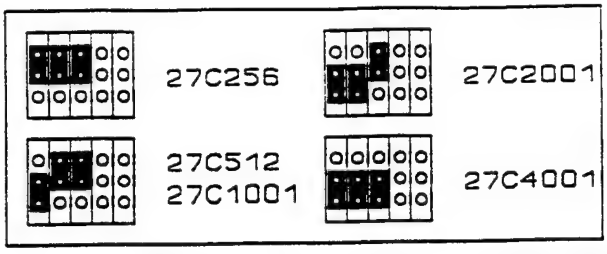
ROM

Sockets **U5** (ROM HI) and **U1** (ROM LO) contain 32k/64k/128k/256k/512k byte wide EPROMs in 0.6" wide DIP packages. Again, two identical ROM devices must be installed.

The figure at the right indicates Jumper J2 positions for the several devices. Once again, the orientation of the diagram is such that the dual-row header P2 would be to the right of the jumper block(s) shown. The table below shows the connections needed to accomodate these choices. "Pin 3", "pin 30" and "pin 31" refer to a 32 pin DIP integrated circuit. In some cases, such as when inserting a 28 pin device into a 32 pin socket, some integrated circuit pins are not connected. This is noted in the table as "nc". The jumper may be left unconnected or, alternatively, tied to +5.



Size	Type	Pin 3	Pin 30	Pin 31
32k	27C256	+5	+5	nc (+5)
64k	27C512	A16	+5	nc (+5)
128k	27C1001	A16	nc(+5)	+5
256k	27C2001	A16	A18	+5
512k	27C4001	A16	A18	A19

EPROM SIZES, TYPES AND VARIANT PIN DESCRIPTIONS

Pins 3 of both EPROMs are connected to the first jumper, pins 30 to the second jumper and pins 31 to the third jumper.

Battery Backed RAM

There are three choices of backup for the onboard RAM; an external battery, the onboard supercap or Dallas Semiconductor Smart Sockets. If an external battery is used, connect an appropriate sized battery pack to **J6** and install a jumper on **J7**. If the onboard supercap is used to supply power to RAM during power down, install a jumper on J7.

J6

Pin	Description
1	Ground (Battery -)
2	External pwr for all RAM (Battery +)

BATTERY BACKUP CONNECTOR

Normally the supercap is used to provide backup power to the 2k bytes of internal RAM in the 68332 microprocessor. The supercap will support internal memory for approximately twenty-four (24) hour. Installing jumper **J7** places the supercap in parallel with the external battery, thus connecting internal RAM to the external battery through a Schottky diode, and also connecting on-board external RAM to the supercap. In this situation, the supercap will preserve the 2k bytes of internal RAM and the two (2) external SRAMs on the SBC332 for approximately eight (8) hours. When a Vesta **MFP332** with realtime clock option installed is connected to an SBC332, the realtime clock is always supercap-backed, regardless of jumpering state. In such cases, the time which the supercap will preserve the 2K bytes internal RAM and the external SBC332 SRAM plus keep the MFP332's reatlime clock running is reduced to one (1) hours.

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Note: *All times given are approximate and conservative and probably vary with individual boards and super-capacitors.*

J7

Pin	Description
1	Supercap
2	RAM socket power

SUPERCAP & BATTERY BACKUP JUMPER

Note: *It is not possible to provide battery backup for 28-pin RAM devices. The battery backup capabilities of the SBC332 are restricted to 32-pin RAM devices.*

The third option for battery backed RAM is to install Dallas Semiconductor DS1213D adaptor sockets into positions U2 and U6. Note that it is not necessary to battery back both sockets if your storage requirements are minimal. The maximum sized memory device that may be installed is limited to 128k bytes per socket due to an internal connection between pins 30 and 32 in the smart socket. This option will, however, battery back 28 pin devices.

Battery Backed Real Time Clock

The Dallas Semiconductor DS1216D may be installed under either RAM socket to provide both battery backed data storage and Real Time Clock function. The same 128k byte limitation exists as with the DS1213D.

Memory Speed

The SBC332 can accomodate many speeds of memory and peripheral devices. The 68332 microcontroller allows all chip selects generated by the 68332 to have up to 13 programmable wait states. When the microcontroller powers up, the boot EPROM's chip select, CSBOOT* is configured for thirteen (13) wait states. Vesta Forth Standard Edition (VFSE) promptly reprograms CSBOOT* and the SRAM chip selects CS0* and CS1* to have three (3) wait states. In conjunction with VFSE's reprogramming of SYNCR, the 68332 Clock Synthesizer Control Register, from the powerup 8.38 MHz to the top rate available (16.777 MHz at this writing), the maximum allowable access time for external memory dictates 200 nS access time devices or better.

If you are using a program development system other than VFSE, the number of wait states programmed into the chip selects and the clock rate programmed into the clock synthesizer circuitry may be under your control, in which case the following discussion still merits your attention.

Access time alone is not the sole determining factor in the timing requirements of the SBC332. The time to "Data Float" is also of concern to prevent bus contention during the *next* bus cycle. The 68332 will deactivate chip selects 15 nS before the end of a memory cycle. The next cycle chip select may be activated as soon as 15 nS into the next cycle. Therefore, peripheral chips must release their data bus drivers within 30 nS, otherwise bus contention may result from the previous cycle's selected chip lingering on the data bus while the currently selected chip is putting its data onto the bus. Usually the EPROMs will be the slowest component in the system to float the data bus. Adding wait states to the next bus cycle will give the bus time to settle down after the contentious period is resolved. Although data float times are generally not a purchasing parameter, it is usually true that the faster the access time, the faster the data float time.

One wait state has a duration of one clock cycle, which is approximately 60 nS at 16.78 MHz. With no wait states inserted, a peripheral must respond within 80 nS of activation of it chip select input. High temperature and low supply voltage worsen CMOS access times. Typical reduction to access times at 4.5

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Volts and 70 degrees C. are as much as 40%. This is mentioned for your information during evaluation only, as published access times are worst case.

Watchdog Timer and Power Supply Monitor

The watchdog timer and power supply monitor will be strobed periodically by CS2* if **J3** pins 1 and 2 are shorted. If CS2* is not strobed every 600 mS the DS1232 will reset the system. This watchdog timer will produce a continuous series of reset pulses until proper operation is restored.

The watchdog timer can be defeated by moving the shorting jumper on jumper J3 to pins 2 and 3. This can be useful during development. In this position, CLKOUT supplies the needed strobe signal.

The power supply monitor will cause a system reset to occur when the +5 supply is 10% or more out of tolerance. The system will be held in reset until proper supply tolerance is restored.

J3

Pin	Description
1	CS2*, output from 68332
2	Watchdog strobe, input to DS1232
3	CLKOUT, output from 68332

WATCHDOG STROBE JUMPER

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Watchdog Timeout Period

Jumper **J9** selects the watchdog timeout period as shown in the diagram.

J9

J9	Period
open	600 ms
1 - 2	1200 ms
2 -3	150 ms

Pushbutton Reset

A pushbutton reset function may be implemented by installing a momentary contact switch at **J4**.

J4

Pin	Description
1	Ground
2	Pushbutton reset input to DS1232

PUSHBUTTON RESET CONNECTOR

Serial Ports

The RS-232-level serial ports are available at **J5**. Port A is assigned to the MC68332 SCI channel. Port B is intended for a software UART implementation. Both channels are brought to RS-232 level by the LT1280 RS-232 transceiver in socket U7.

J5

Pin	I/O	Description
1	O	TxDA - RS-232
2	GND	GroundA
3	I	RxDA - RS-232
4	O	TxDB - RS-232
5	GND	GroundB
6	I	RxDB - RS-232

RS-232 SERIAL PORT CONNECTOR

Jumper J10 and Software Control of Serial Transceiver

Jumper **J10** when installed allows **TPU Channel 5** to enable and disable the serial transceiver under software control: when TPU5 is set logic-high, the LT1280 is enabled; when TPU5 is set low under software control, the LT1280 is disabled. (This feature is especially useful in conjunction with low-power operation, since the LT1280 enabled can draw current in the vicinity of 10 mA, as opposed to somewhat more than

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1 µA disabled.) Should it be desirable in the context of an application to use TPU Channel 5 for another purpose, jumper J10 may be removed, in which case the serial transceiver is automatically enabled by a pullup resistor. ***Note:*** *The SBC332 is shipped with jumper J10 removed. If jumper J10 is installed during development, please note that the powerup default of the MC68332 microcontroller is TPU5 low.*

Second Software Serial Port and Jumper J12

TPU Channel 4 serves as the Port B TxD input to the LT1280 RS-232 transceiver. **TPU Channel 1** serves as the Port B RxD output. Vesta Forth Standard Edition features a full-source implementation of a second serial port utilizing these TPU channels.

Should it be desirable in the context of an application to use TPU Channels 1 and 4 for another purpose, losing use of the second asynchronous serial port, jumper **J12** may be removed. Removing jumper J12 disconnects the transceiver output from TPU Channel 4. (It is not necessary to disconnect the transceiver input from TPU Channel 1 in order to be able to use TPU Channel 1 for a task other than the second asynchronous serial port.)

Background Mode Connector

J8 is available as the Motorola standard debugging interface.

J8

Pin	I/O	Description
1	I	Ground
2	I	DSCLK
3	I	Ground
4	O	QUOT
5	I/O	RESET*
6	O	DSI
7	O	Vcc
8	O	DSO

BACKGROUND MODE CONNECTOR

BCC Connectors

Every attempt has been made to conform to the standard set by Motorola's BCC (Business Card Computer) pinout. The only differences which exist are in the areas of programming the system EPROM in-place (which is impossible on the SBC332). The following tables show the pinouts of the two principal offboard connectors (P1 and P2) on the SBC332.

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P1

Pin	I/O	Description	Pin	I/O	Description
1	-	Ground	2	-	Ground
3	-	Vcc	4	-	Vcc
5	-	no connection	6	O	A0
7	O	A1	8	O	A2
9	O	A3	10	O	A4
11	O	A5	12	O	A6
13	O	A7	14	O	A8
15	O	A9	16	O	A10
17	O	A11	18	O	A12
19	O	A13	20	O	A14
21	O	A15	22	O	A16
23	O	A17	24	O	A18
25	-	no connection	26	-	no connection
27	-	no connection	28	I	VSTBY
29	-	no connection	30	I	T2CLK
31	I/O	TP15	32	I/O	TP14
33	I/O	TP13	34	I/O	TP12
35	I/O	TP11	36	I/O	TP10
37	I/O	TP9	38	I/O	TP8
39	I/O	TP7	40	I/O	TP6
41	I/O	TP5	42	I/O	TP4
43	I/O	TP3	44	I/O	TP2
45	I/O	TP1	46	I/O	TP0
47	O (I)	MOSI	48	I (O)	MISO
49	O	PCSO	50	O	SCK
51	O	PCS2	52	O	PCS1
53	O	TxD	54	O	PCS3
55	I	DSCK	56	I	RxD
57	I/O	RESET*	58	O	QUOT
59	O	DSO	60	O	DSI
61	-	VCC	62	-	VCC
63	-	GND	64	-	GND

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P2

Pin	I/O	Description	Pin	I/O	Description
1	-	Ground	2	-	Ground
3	-	Vcc	4	-	Vcc
5	I/O	D1	6	I/O	D0
7	I/O	D3	8	I/O	D2
9	I/O	D5	10	I/O	D4
11	I/O	D7	12	I/O	D6
13	I/O	D9	14	I/O	D8
15	I/O	D11	16	I/O	D10
17	I/O	D13	18	I/O	D12
19	I/O	D15	20	I/O	D14
21	-	no connection	22	-	no connection
23	-	no connection	24	O	XMT232
25	O	CSBOOT*	26	I	RCV232
27	O	R/W*	28	I	MODCK
29	I	TSC	30	O	CS10*
31	O	CS9*	32	O	CS8*
33	O	CS7*	34	O	CS6*
35	O	CS5*	36	O	CS4*
37	O	CS3*	38	O	CS2*
39	O	CS1*	40	O	CS0*
41	I	IRQ1*	42	I	IRQ2*
43	I	IRQ3*	44	I	IRQ4*
45	I	IRQ5*	46	I	IRQ6*
47	I	IRQ7*	48	I	BERR*
49	I	DSACK0*	50	I	DSACK1*
51	I	AVEC*	52	O	RMC*
53	O	DS*	54	O	AS*
55	O	SIZ0	56	O	SIZ1
57	-	no connection	58	O	CLKOUT
59	-	no connection	60	I/O	HALT*
61	-	Vcc	62	-	Vcc
63	-	Ground	64	-	Ground

Pin Usage Differences

The following pins differ in usage between the Motorola BCC and the Vesta Technology SBC332:

1. On connector **P1**, pins 25, 26, 27, and 29 are unconnected on the SBC332. On the BCC, they are used to provide the capability of programming the system EPROM in-place.

2. On connector **P2**, pins 21, 22, 23, and 57 are unconnected on the SBC332. On the BCC, they provide an interface via the platform board (PFB) to the BCCDI, a 68HC11-based single-board computer which also attaches to the PFB.

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Other Differences between the Motorola BCC and the SBC332

Besides the connector differences mentioned elsewhere, the SBC332 uses a different configuration of chip select signals for accessing on-board RAM than is used by the BCC. The BCC controls all RAM read and write accesses using three chip-select lines: CS0* CS1* and CS2*. The SBC332 uses the processor's R/W* signal for selecting read or write accesses to RAM, and therefore only required CS0* and CS1* for chip selection.

The specific configuration differences are as follows:

Signal	Board	Usage
CS0*	BCC SC332	Write access to the upper byte of a word. Read and write access to the upper byte of a word.
CS1*	BCC SBC332	Write access to the lower byte of a word. Read and write access to the lower byte of a word.
CS2*	BCC SBC332	Read access to both bytes of a word. Not used.

CHIP SELECT VARIANCE BCC <> SBC332

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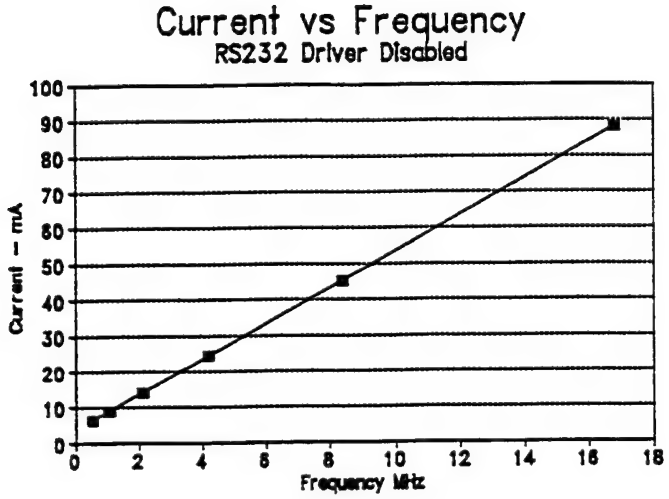
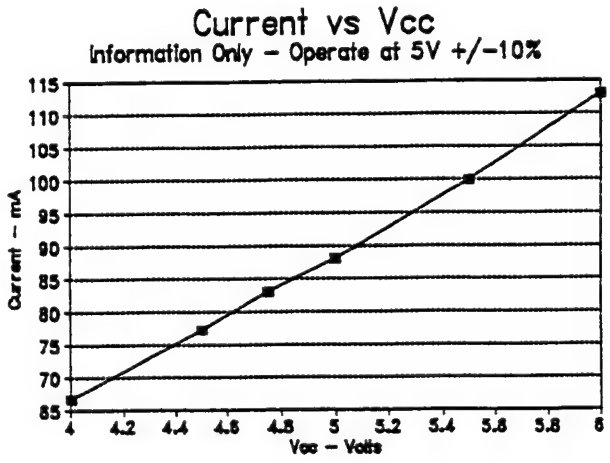
Power Consumption

The power requirement of the SBC332 is largely a function of the clock frequency. The graph titled **Current vs Frequency** shows this relationship at Vcc = 5.00 Volts. This data was obtained from a single unit of the latest revision of Motorola's MC68332. Earlier revisions of this microprocessor have evidenced up to 50% higher currents. The RS-232 driver was disabled during this test.

Entering low power stop mode decreases the current drain to less than 2 mA. Note that the external watchdog strobe will stop if the oscillator is stopped causing the system to be reset at the watchdog timeout period. If the watchdog input source is CLKOUT then the watchdog will not reset the board as long as the oscillator is running. During all modes of low power operation it is important that all inputs to P1 and P2 be terminated with pullup resistors. Unless this is done, up to 20 mA of leakage currents will be observed.

The power requirement is also a weak function of Vcc as shown in the graph titled **Current vs Vcc**. Please note that although the SBC332 appears to operate from 4 Volts to 6 Volts, the Vcc specification for all of the components is 4.75 Volts to 5.25 Volts.





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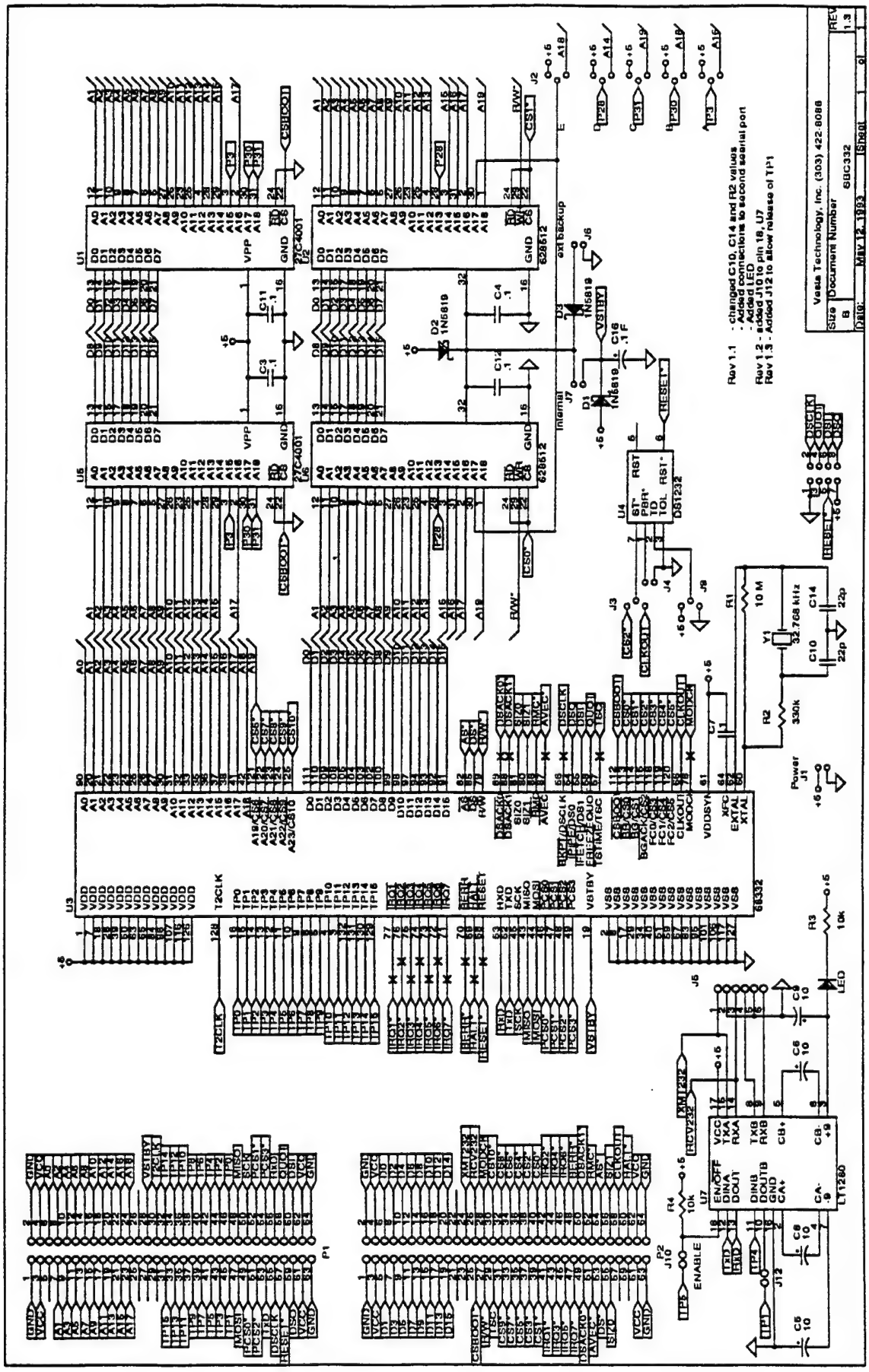

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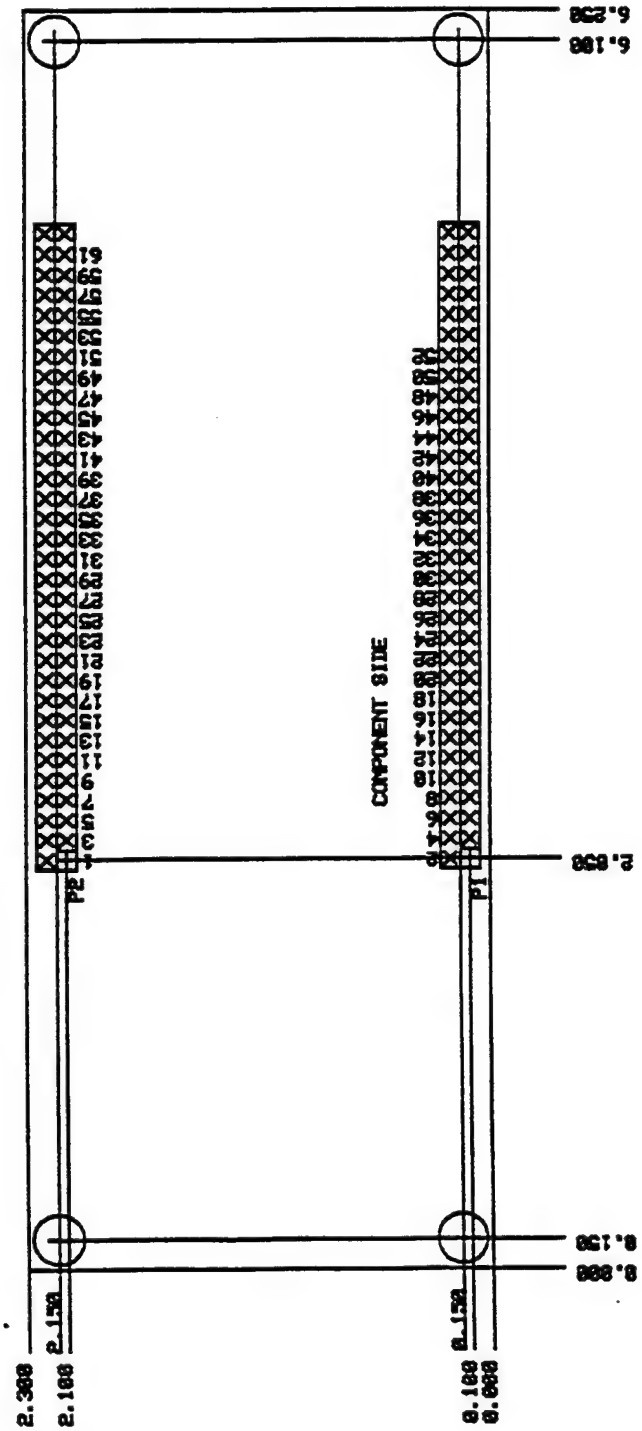

Size and Mounting

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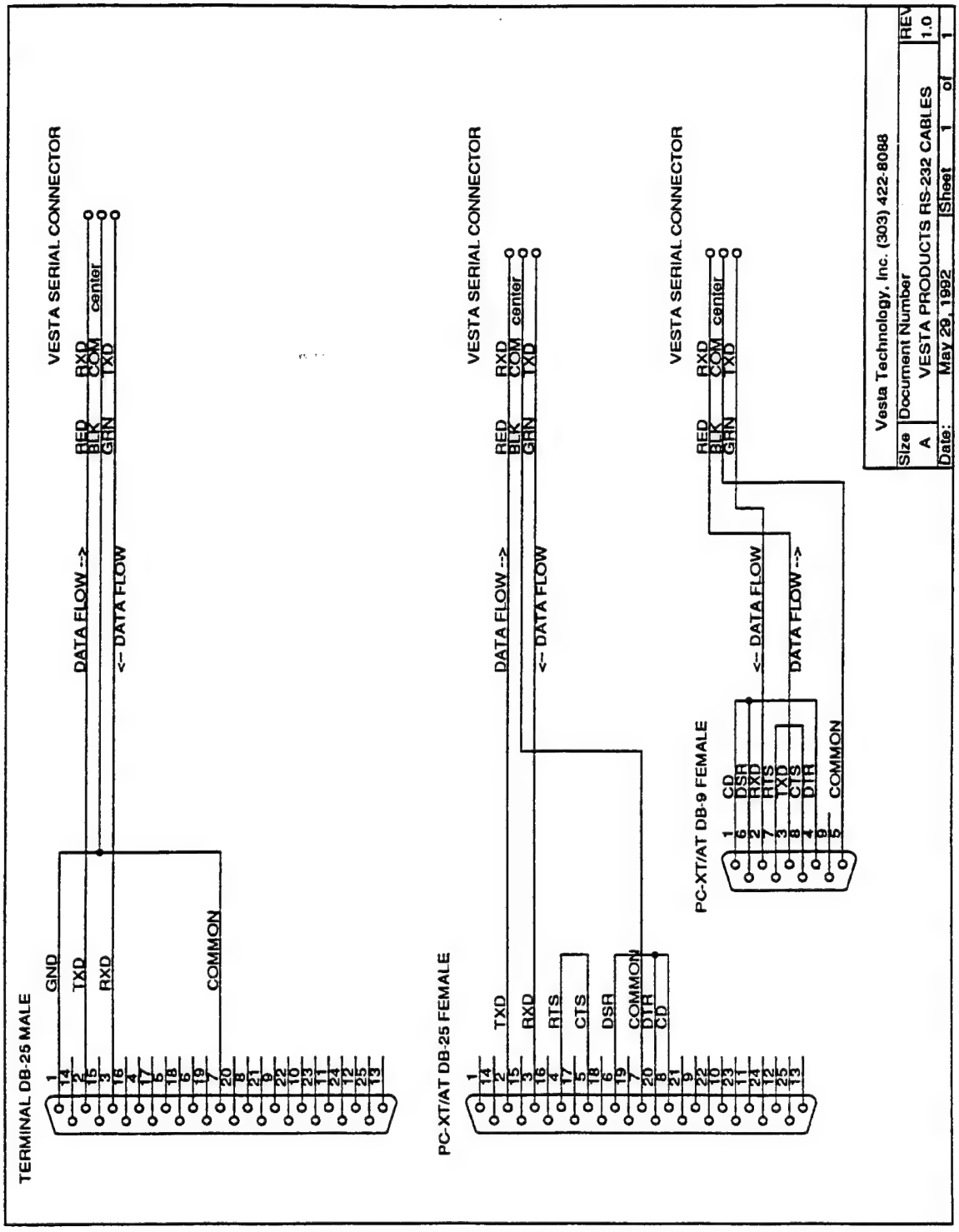
RS-232 Cabling Diagram



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AD9955/PCB DDS Evaluation Board

AD9955/PCB

FEATURES
IBM-Compatible PC for Test Control
Standard Centronics Printer Cable
SMB Connectors on Analog and Clock Inputs/Outputs
Evaluates AD9713B and AD9721
Test Software Included

GENERAL DESCRIPTION

The AD9955/PCB DDS Evaluation Board allows designers to evaluate the high performance AD97xx D/A Converters with a minimum amount of effort.

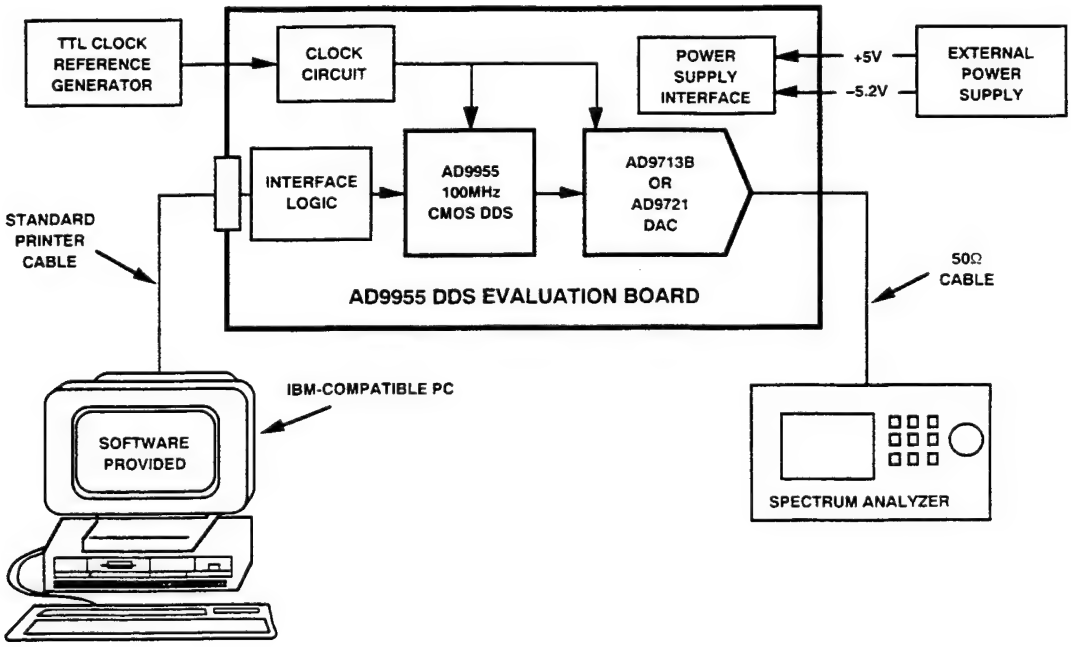
To prove these DACs will meet the user's waveform synthesis requirements, the only things needed are the AD9955/PCB DDS Evaluation Board, +5 V/−5.2 V power supplies, an IBM-compatible PC, a spectrum analyzer, and a TTL signal generator. The evaluation setup is shown below.

The DDS evaluation kit includes a populated, tested AD9955/PCB board; software which controls the tuning word for the input frequency through the parallel printer port; and one sample each of the AD9713B and AD9721 DACs.

The AD9713B and AD9721 are TTL-compatible DACs designed specifically for DDS, waveform reconstruction, and high resolution imaging applications. The AD9713B is a 12-bit, 80 MSPS device; the AD9721 is a 10-bit, 100 MSPS DAC. Both units feature low glitch and outstanding dynamic performance.

Testing of the DACs can be done by alternately installing them in sockets on the board; a model AD9955 Direct Digital Synthesizer is soldered in place.

The AD9955 is a CMOS 100 MHz device for frequency synthesis applications. It comprises a 32-bit phase accumulator and a 15-bit phase-to-12-bit-sine amplitude converter. Its control logic is CMOS compatible, and the clock input is TTL. CMOS outputs are latched on board and a data ready signal is available.



AD9955 DDS Evaluation Board Setup

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AD9955/PCB—SPECIFICATIONS

Typical Electrical Characteristics (Nominal power supplies; AD9721 installed; CLK = 80 MHz)

Characteristic	Typical Value	Units
−5.2 VD (Digital) Supply Current (TP1)	270	mA
−5.2 VA (Analog) Supply Current (TP2)	30	mA
+5.0 V Supply Current (TP3)	250	mA
AD9713B Output Voltage (J3 or J4, Terminated into 50 Ω Externally)	0 to −0.5	V
AD9721 Output Voltage (J5 or J6, Terminated into 50 Ω Externally)	0 to −0.5	V
TTL clock input HIGH (J2)	2.4 to 5	V
TTL clock input LOW (J2)	0.0 to 0.5	V

Using the AD9955/PCB DDS Evaluation Board

The AD9955/PCB evaluation kit is a test system designed to simplify the evaluation of the AD9713B 12-bit, 80 MSPS TTL DAC or the AD9721 10-bit, 100 MSPS TTL DAC when either is driven by the AD9955 100 MHz Direct Digital Synthesizer. Provisions to control the AD9955 from the printer port of an IBM-compatible PC are included, along with the necessary software. This data sheet provides information on operating the evaluation board; additional details are available from ADI/CLG Applications Engineering: (919) 668-9511.

Choosing a DAC

A sample of each DAC (AD9713BBN and AD9721BN, both are PDIPs) is included with the AD9955/PCB. One or the other is installed in the evaluation board by the user. The analog outputs of the DACs are available through SMB connectors (J3–J6). Cables and adapters for these connectors are available from Pasternack Enterprises [(714) 261-1920].

It is suggested that both DAC designs be evaluated to determine which converter will provide optimum performance (highest Spurious Free Dynamic Range) in the final application. The AD9713B fits into the pin sockets of U9, while the AD9721 fits into the pin sockets of U10. The DACs can be installed only one at a time since they share area in the layout.

Warning: Since both DACs are in 28-pin PDIPs, users should take care not to install the DAC in the wrong socket. Installation of either DAC in the wrong socket can result in device failure. Power should be off when installing the devices.

In general, the AD9713B will provide the best performance in applications which use update rates below 20 MSPS and analog output frequencies below 5 MHz. These applications tend to be limited by the linearity of the converter and will benefit from the 12-bit resolution of the AD9713B. Applications which use faster clock rates or generate analog outputs higher than 5 MHz will benefit from the ultralow switching transients of the AD9721.

Prototyping Area

An area near one edge of the board (marked "PROTO AREA") is intentionally left void of components to allow the user to add additional circuits to the evaluation test set. The wide strip on both sides of the PWB is connected to the internal ground plane, and the through holes are electrically isolated. J7 and J8 are provided to add additional SMA or SMB connectors for analog signals. Users may want to build custom analog filters for the DAC outputs, or add buffers and operational amplifiers used in the final applications.

XO vs. External Clock

The reference clock of the AD9955/PCB is normally provided by an external TTL signal applied to connector J2. This SMB connector is terminated into 50 Ω by R13. If desired, R13 can be removed and a standard TTL crystal oscillator can be installed in DIP socket Y1 to improve performance and/or simplify the evaluation process.

The reference clock is hardwired to the AD9955. Strap options installed during assembly also connect the reference clock directly to the clock inputs of the DACs (see E2–E4 below). The user may opt to remove these straps and clock the DACs with the data ready signal (DRDY) of the AD9955 (E1), or provide an external TTL compatible signal.

Power Supplies

Power for the AD9955/PCB must be provided externally through the pin connections TP1–TP4, as described in the Inputs/Outputs. It is suggested that the user solder leads to these pins and connect them to a low impedance, low noise, linear power supply. Two isolated holes of 0.15″ diameter are located between the test points and the edge of the board; these can be used for wire wraps to provide stress relief for the power leads.

Current levels through the supplies are shown in the specification table. Although analog and digital −5.2 V power supplies are separated (this provides best performance), the user may opt to connect the two supplies during evaluation.

Controlling the AD9955/PCB

The AD9955/PCB is designed to allow control (frequency specification, reset, etc.) through the parallel printer port of a standard IBM-compatible PC. The user simply disconnects the printer cable from the printer and inserts it into edge connector J1 of the evaluation board.

The printer port provides information to the AD9955/PCB through eight data lines and two control lines. Data is latched into registers on the AD9955/PCB (U1–U7) and transferred to the AD9955.

A 5.25″ floppy disk containing software to control the AD9955 is provided with the AD9955/PCB. This software was developed using Quick Basic from Microsoft, Inc. The original Quick Basic source code is provided in a file named A:\AD9955.BAS, which the user may view, run, or modify with the Quick Basic Software (not provided, available from Microsoft).

An executable version of this software is also provided, and can be executed from DOS by typing "a:\ad9955." The software prompts the user to provide the necessary information needed by the program. Additional information is included in a text file named a:\readme.doc.

AD9955/PCB BILL OF MATERIAL

Quantity	Description	Circuit Designation
6	Terminals	TP1–TP6
60	Pin Sockets (U9, U10, Y1)	NA
5	SMB PC Mount Connectors	J2–J6
1	36-Pin PC-Mount Connector	J1
28	0.1 μF Chip Capacitors (Size 0805)	C1, C3–C6, C10–C11, C13–C22, C24–C27, C30–C32, C50–C53
3	10 μF Capacitors	C23, C29, C33
12	130 Ω Chip Resistors	R1–R12
5	49.9 Ω Chip Resistors	R13, R18, R19, R21, R22
1	20 Ω Chip Resistor	R16
1	2 kΩ Chip Resistor	R14
1	7.5 kΩ Chip Resistor	R17
7	ALS 574 Octal Flip-Flops (SOIC)	U1–U7
1	AD9955KS Direct Digital Synthesizer	U8
1	AD9713BBN	U9
1	AD9721BN D/A Converter	U10

ORDERING GUIDE

Catalog Number	Description
AD9955/PCB	AD9955/PCB DDS Evaluation Kit, Assembled and Tested
AD9955/PWB	AD9955/PWB DDS Evaluation Board, PWB Only

Inputs/Outputs

Name	Description
J1	36-pin edge connector designed to mate with parallel printer port of IBM-compatible PC. Software provided with the AD9955/PCB allows the user to load data from a PC into the AD9955.
J2	SMB connector for external TTL input; R13 provides 50 Ω termination.
J3	SMB connection to the analog output of the AD9713B (U9, I_{OUT}, Pin 14).
J4	SMB connection to the complementary analog output of the AD9713B (U9, $\overline{I_{OUT}}$, Pin 16).
J5	SMB connection to the analog output of the AD9721 (U10, I_{OUT}, Pin 20).
J6	SMB connection to the complementary analog output of the AD9721 (U10, I_{OUT}, Pin 21).
J7/J8	Optional locations for SMB connectors near prototyping area (connectors not included).
TP1	Pin connection for external −5.2 V digital power supply; nominally 270 mA.
TP2	Pin connection for external −5.2 V analog power supply; nominally 30 mA.
TP3	Pin connection for external +5 V power supply; nominally 250 mA with 80 MHz clock.
TP4	Pin connection for external ground reference.
TP5	Pin connection to monitor carry out (C_{OUT}) signal of AD9955 (Pin 61).
TP6	Optional pin connection for external −5.2 V analog power supply. Can be used to connect −5.2 V analog supply near DACs; not necessary to drive this pin under normal conditions.
E1	Optional through hole connection to data ready (DRDY) signal of the AD9955 (Pin 62).
E2	Through hole connection to the LATCH ENABLE (Pin 26) of the AD9713B; normally connected to E4 with external strap.
E3	Through hole connection to the CLOCK (Pin 11) of the AD9721; normally connected to E4 with external strap.
E4	Through hole connection to the master clock of the AD9955/PCB DDS Evaluation Board. Master clock may be provided by a user-installed TTL crystal oscillator (Y1) or an external TTL signal applied to J2.

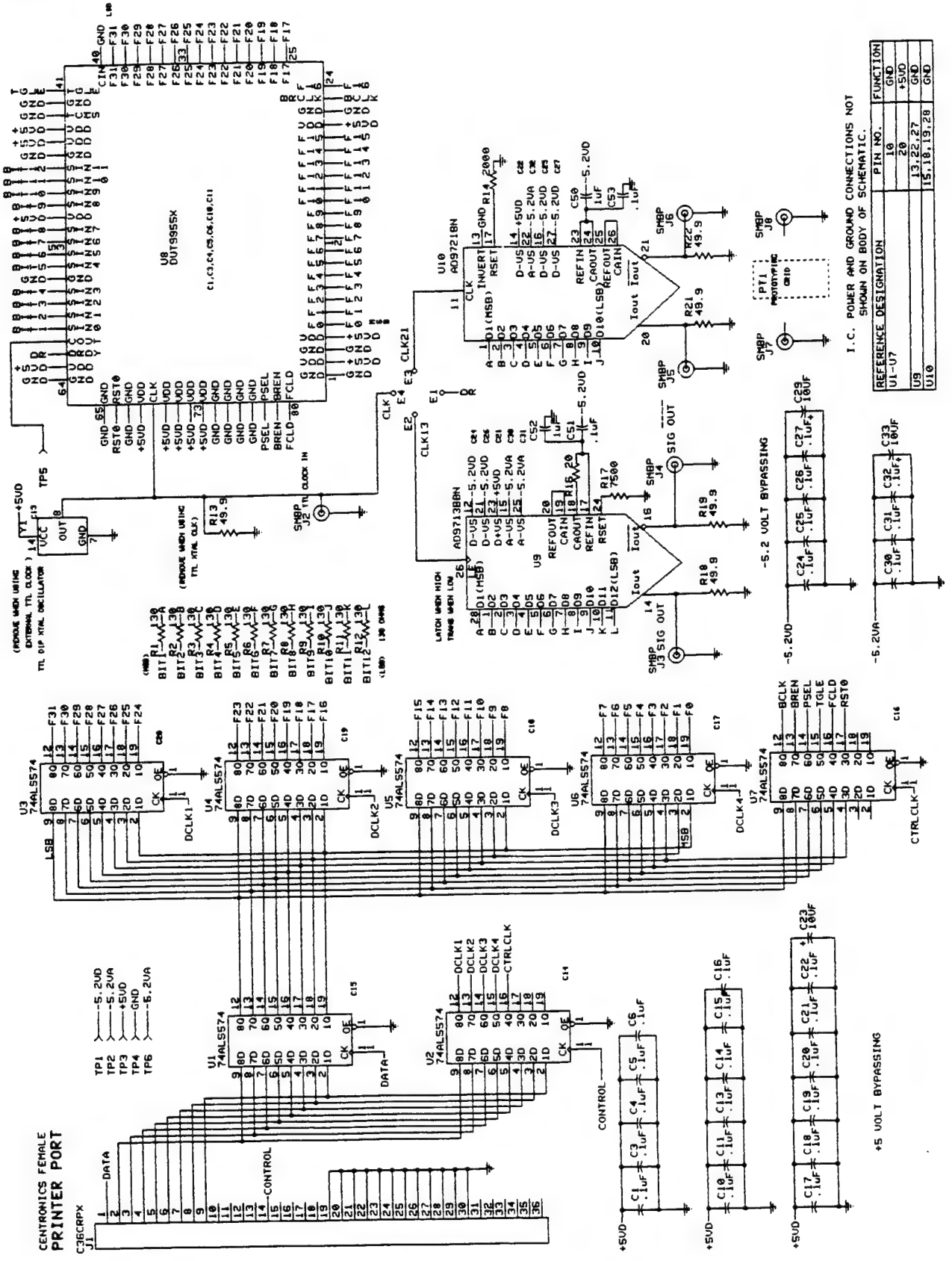

Figure 1.

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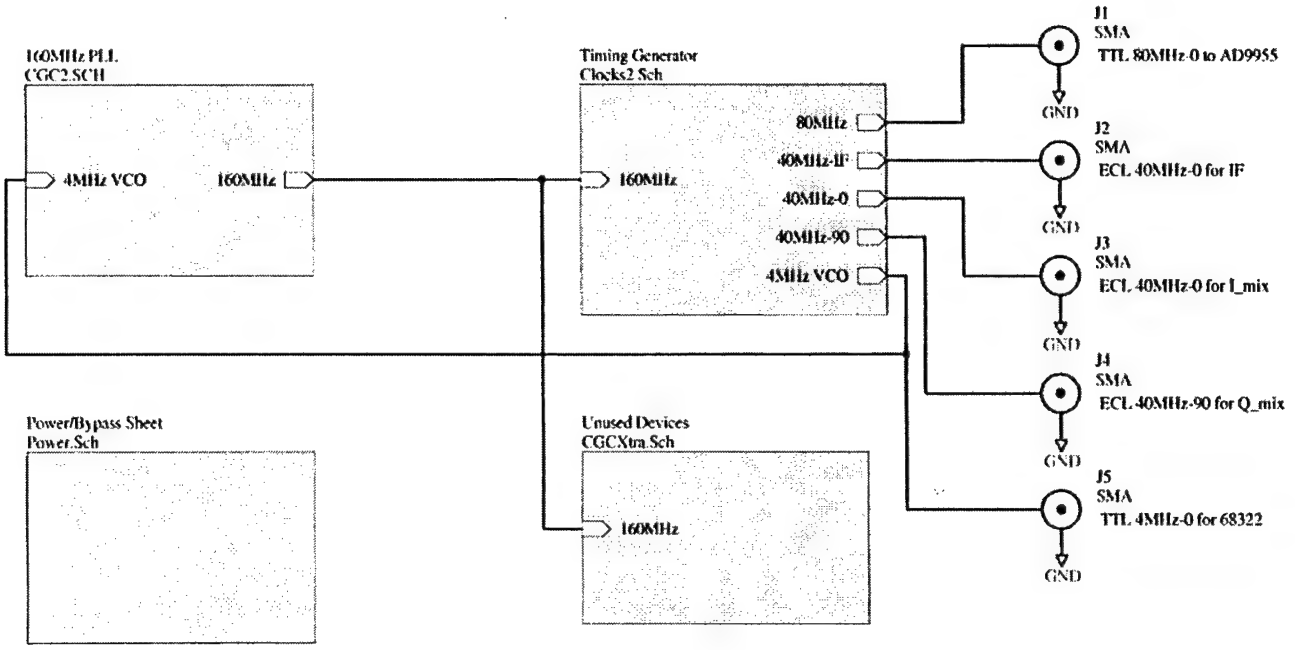
SYSTEM DOCUMENTATION
(ERIM)



Originator

ERIM

Title
HF Radar Clock Generator Circuit - Mark II

Size: A | Number: | Revision: C

File: D:\PROJECTS\HFRADAR\HF_CGC2.PRJ | Date: 21-May-1997 Time: 16:04:48 | Sheet 1 of 5

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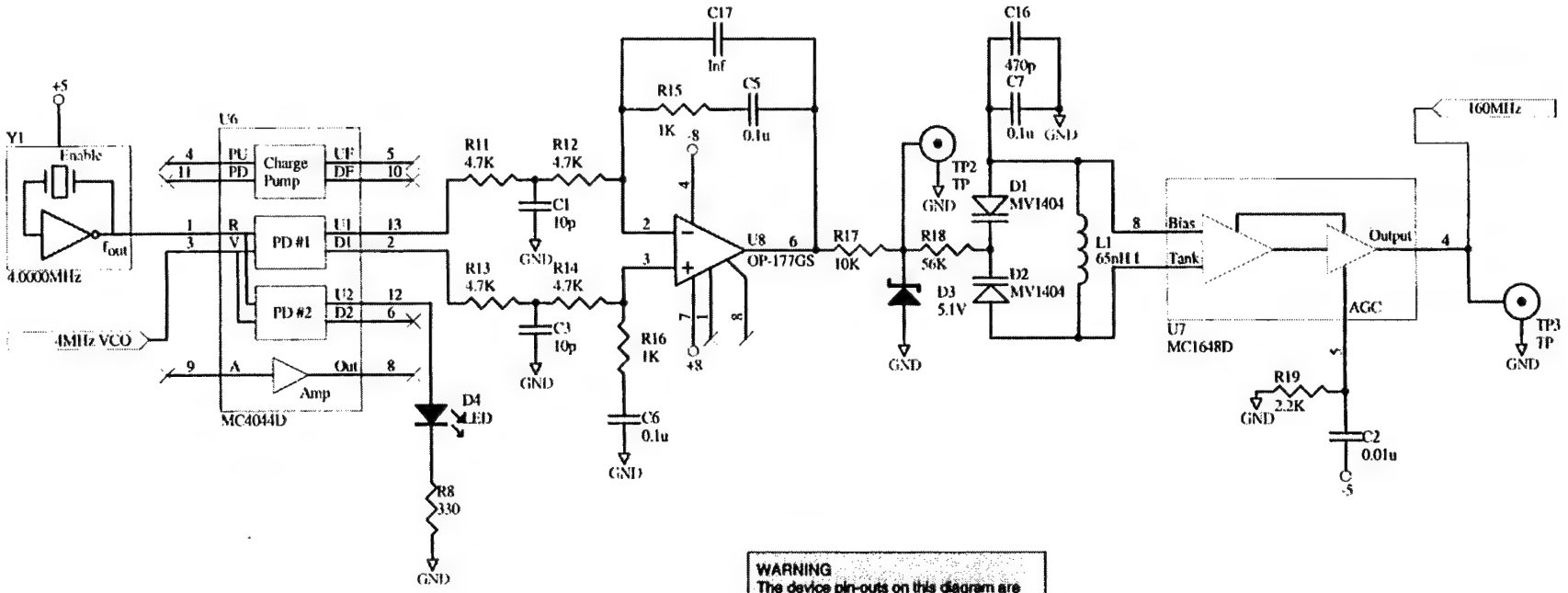
United States of America

Note: C17 is a place-holder.



WARNING
The device pin-outs on this diagram are for surface-mount parts and are NOT to be used for wire-wrapping or breadboarding purposes. Refer to the proper datasheet for each device to obtain the standard part pinouts.

Originator

ERIM

Title: *HF-Radar CGC 160 MHz PLL - Mark II*

Size: A | Number: | Revision: C

File: CGC2.SCH | Date: 21-May-1997 Time: 16:04:56 | Sheet 2 of 5

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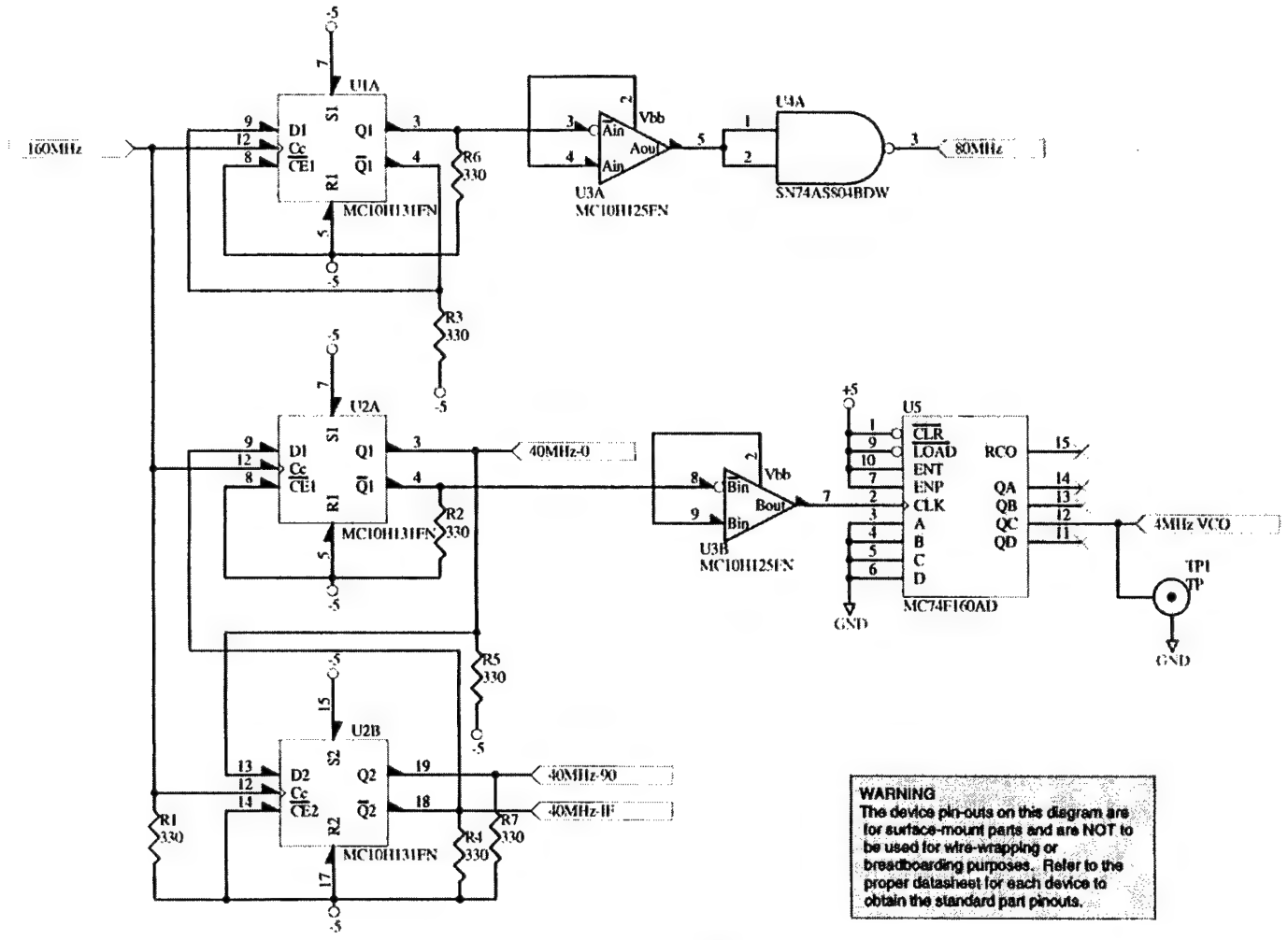

WARNING
The device pin-outs on this diagram are for surface-mount parts and are NOT to be used for wire-wrapping or breadboarding purposes. Refer to the proper datasheet for each device to obtain the standard part pinouts.

Originator

ERIM

Title
HF-Radar CGC Clk Division Unit - Mark II

Size: A | Number: | Revision: C

File: CLOCKS2.SCH | Date: 21-May-1997 Time: 16:05:19 | Sheet 3 of 5

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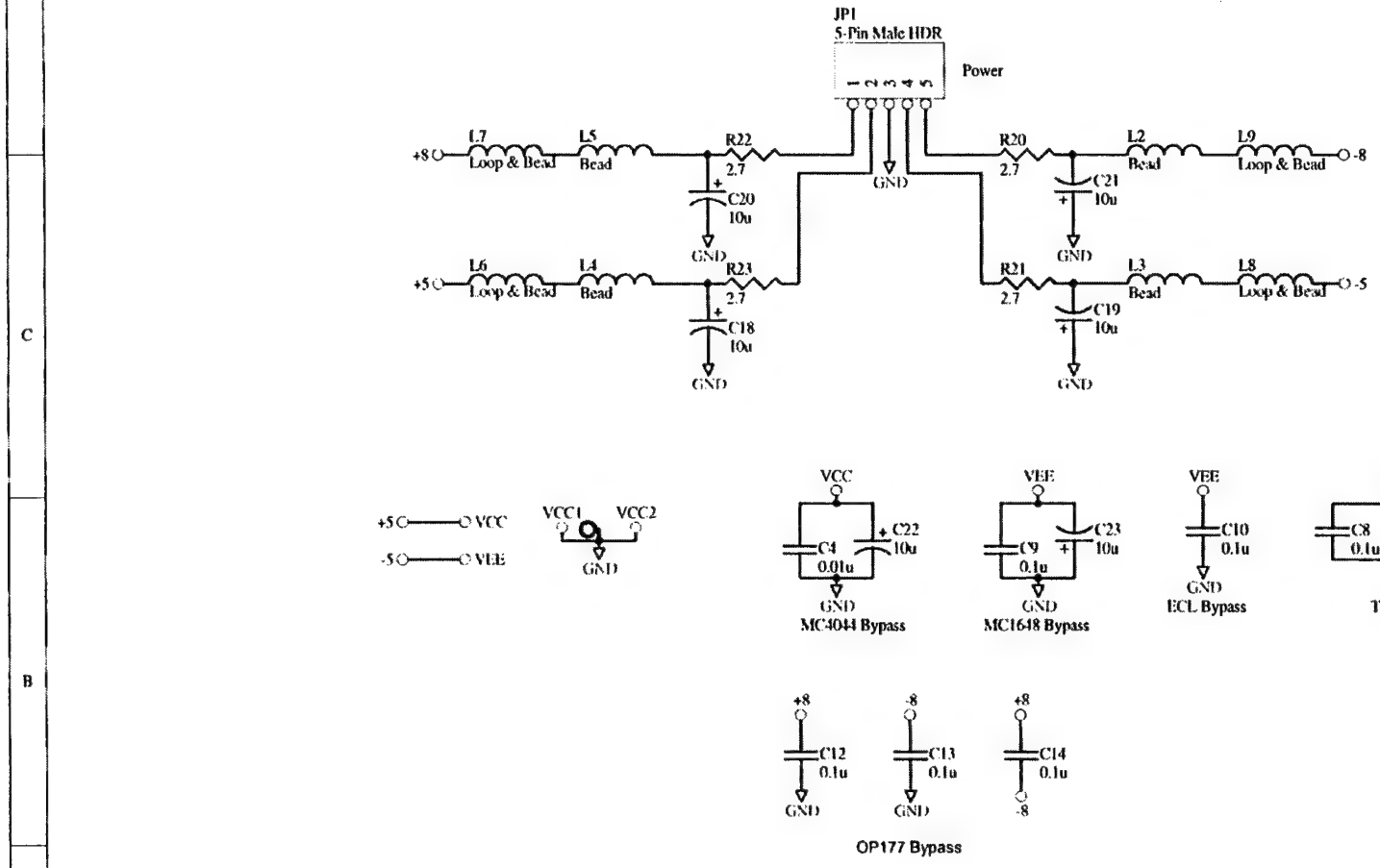

Originator

ERIM

Title
HF-Radar CGC Power Distribution

Size: A | Number: | Revision: C

File: POWER.SCH | Date: 21-May-1997 Time: 16:05:08 | Sheet 4 of 5

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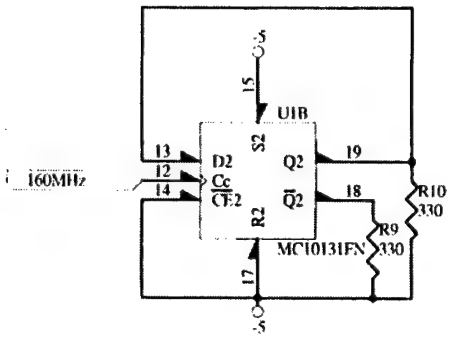

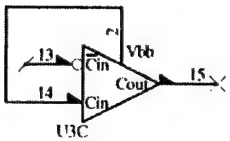

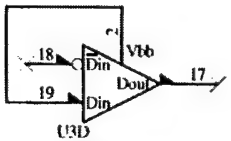

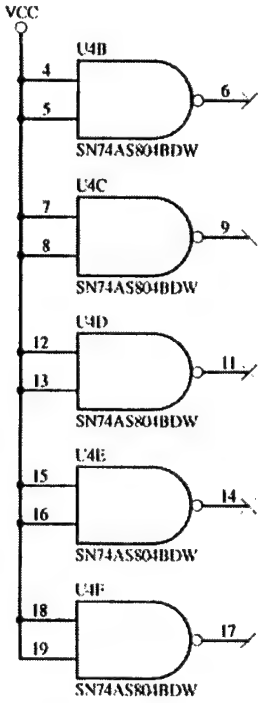

WARNING
The device pin-outs on this diagram are for surface-mount parts and are NOT to be used for wire-wrapping or breadboarding purposes. Refer to the proper datasheet for each device to obtain the standard part pinouts.

Originator

ERIM

Title
HF-Radar CGC Unused Devices

Size: A	Number:	Revision: C
File: CGCXTRA.SCH	Date: 21-May-1997 Time: 16:05:30	Sheet 5 of 5

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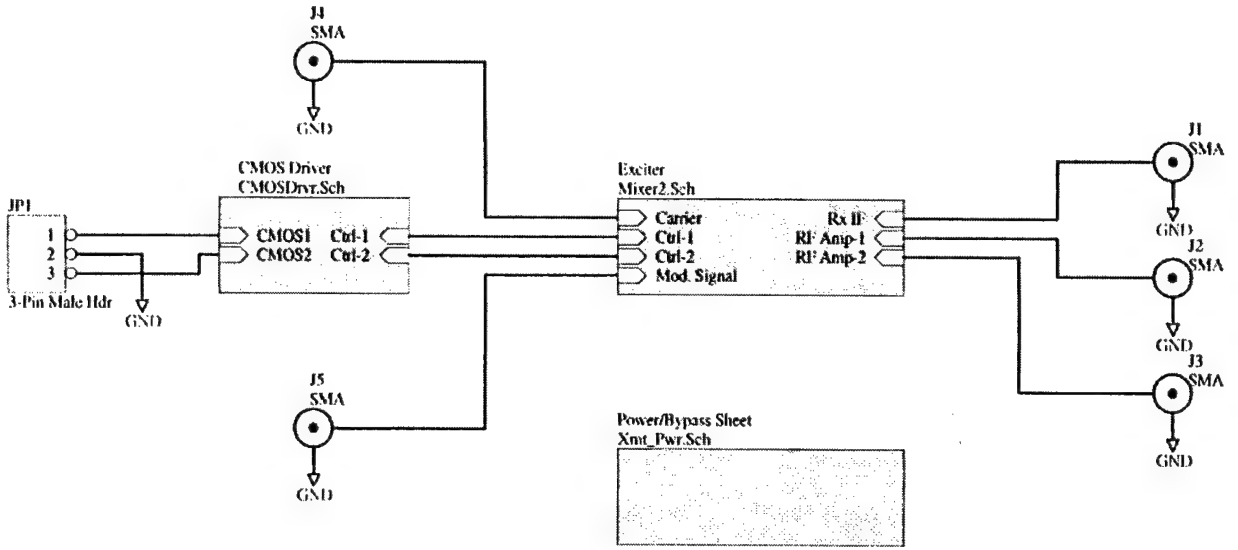

Originator

ERIM

Title
HF Radar Exciter Module

Size: A | Number: | Revision: E

File: D:\PROJECTS\HFRADAR\EXCITER.PRJ | Date: 21-May-1997 Time: 15:28:49 | Sheet 1 of 4

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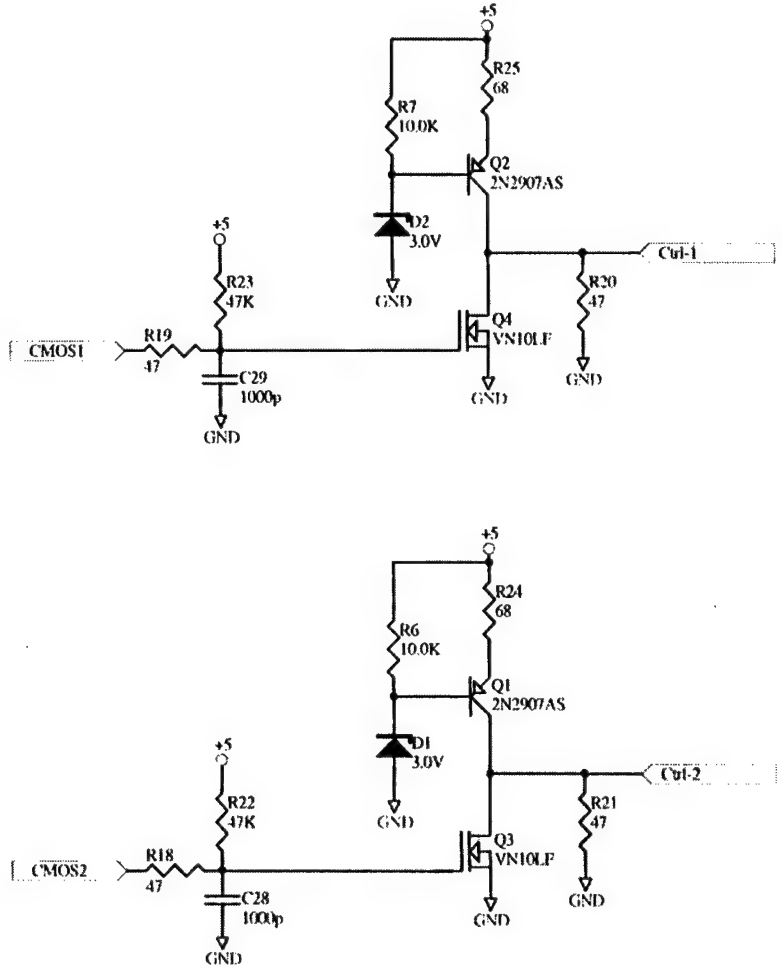

Originator

ERIM

Title
HF-Radar Exciter TFAS Ctrl Driver

Size: A | Number: | Revision: E

File: D:\PROJECTS\HFRADAR\CMOSDRVR.SCH Date: 21-May-1997 Time: 15:29:07 | Sheet 2 of 4

ERIM
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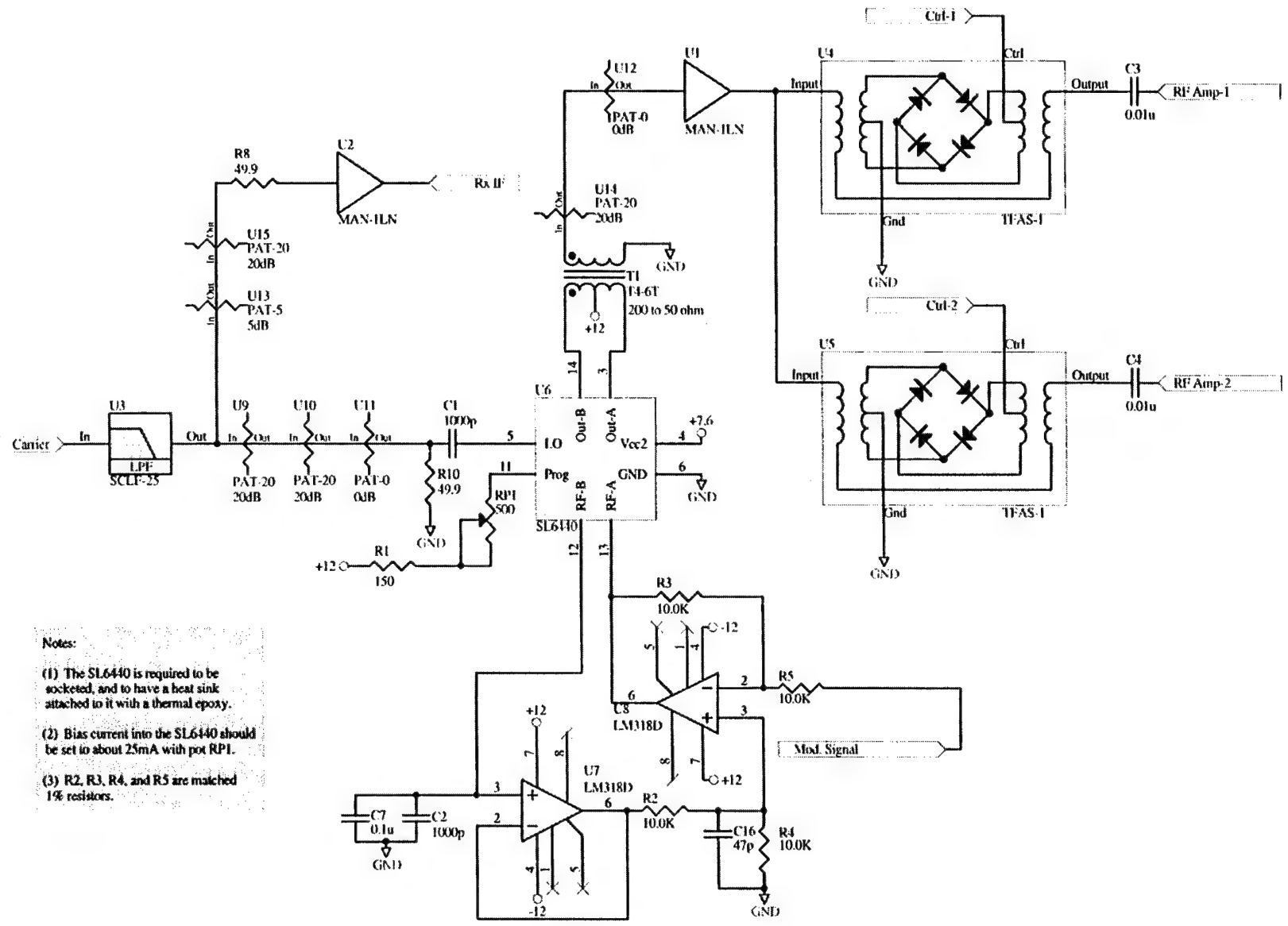

Notes:

(1) The SL6440 is required to be socketed, and to have a heat sink attached to it with a thermal epoxy.

(2) Bias current into the SL6440 should be set to about 25mA with pot RP1.

(3) R2, R3, R4, and R5 are matched 1% resistors.

Originator

ERIM

Title
HF Radar Exciter Circuit

Size: A | Number: | Revision: E

File: D:\PROJECTS\HF\RADAR\MIXER2.SCH | Date: 21-May-1997 Time: 15:36:13 | Sheet 3 of 4

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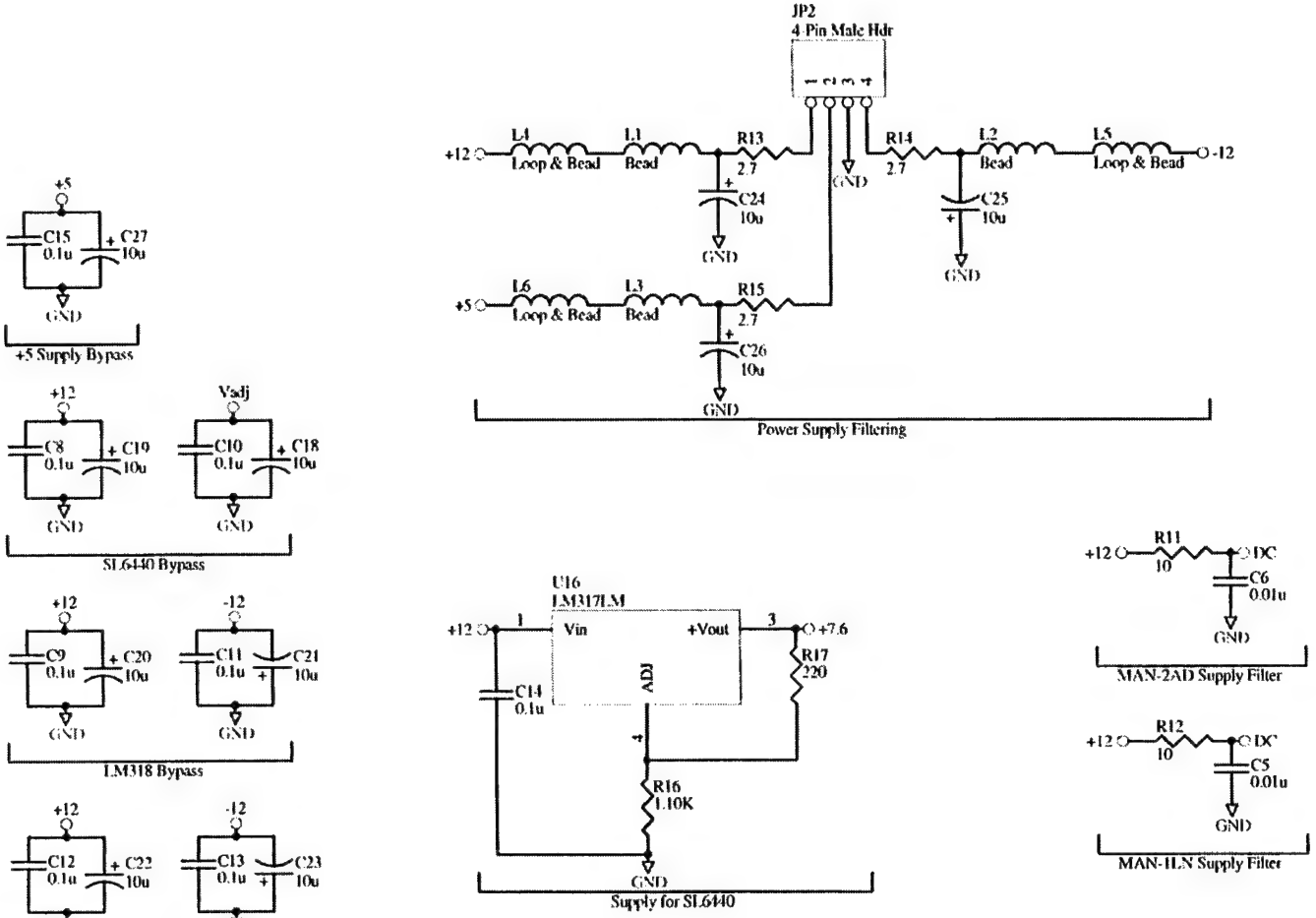
United States of America



Originator

ERIM

Title
HF Radar Exciter Power Distribution

Size: A | Number: | Revision: E

File: D:\PROJECTS\HF-RADAR\XMT_PWR.SCH Date: 21-May-1997 Time: 15:29:25 | Sheet 4 of 4

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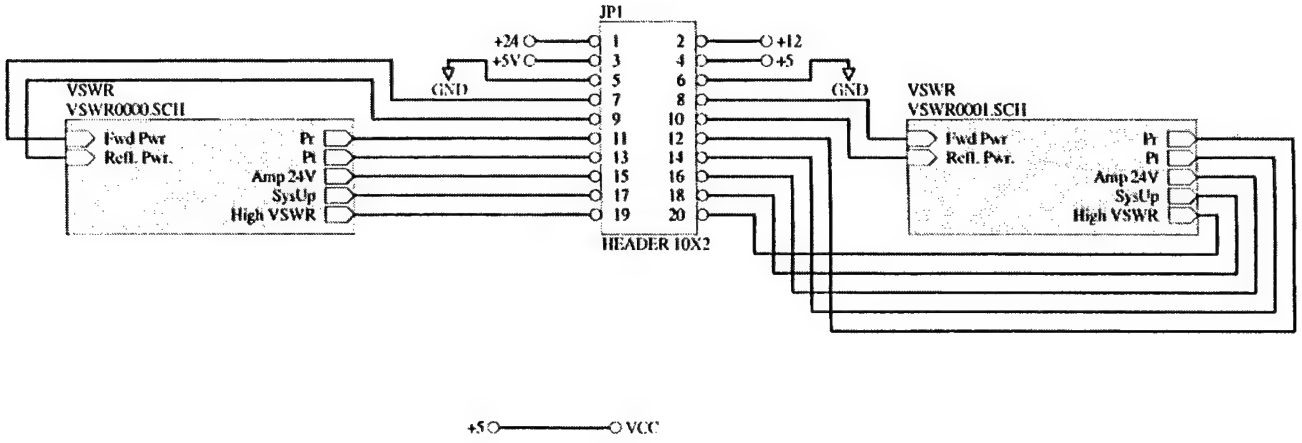

Originator

ERIM

Title
VSWR Protection Circuit

Size: A | Number: | Revision: B

File: D:\PROJECTS\HFRADAR\VSWRTRIP.PR | Date: 21-May-1997 Time: 16:06:10 | Sheet 1 of 3

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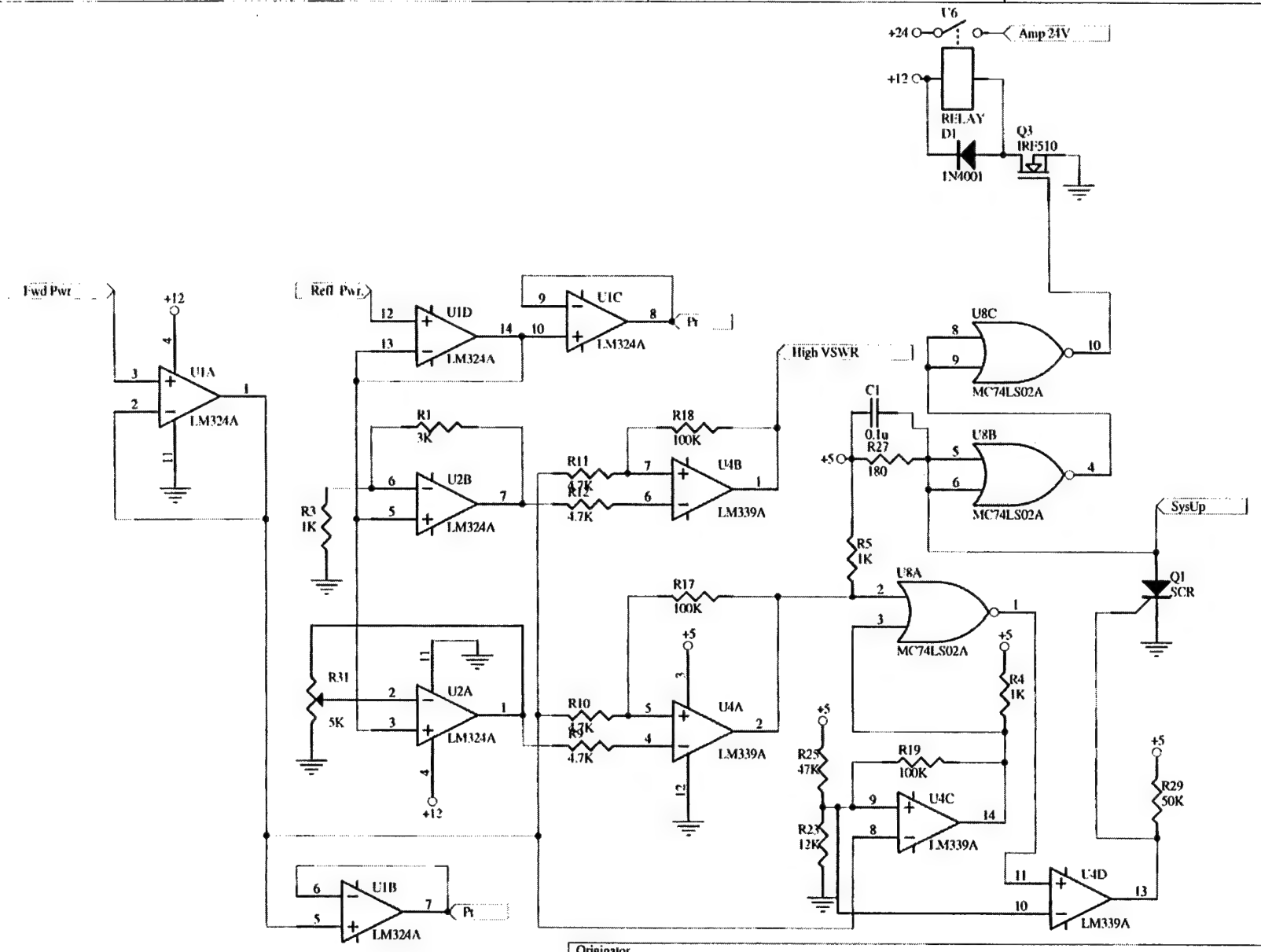
U6
+24
Amp 24V
+12
RELAY
D1
1N4001
Q3
IRF510
Fwd Pwr
Refl Pwr
+12
U1A
LM324A
U1D
U1C
Pf
High VSWR
U8C
MC74LS02A
C1
0.1u
R27
180
U8B
R1
3K
R18
100K
R11
4.7K
R12
4.7K
U2B
U4B
LM339A
R3
1K
R5
1K
U8A
SysUp
Q1
SCR
R17
100K
R31
5K
U2A
R10
4.7K
R9
4.7K
U4A
R4
1K
R25
47K
R19
100K
U4C
R23
12K
R29
50K
U1B
U4D
Pr
Originator
ERIM
Title
VSWR Trip Subcircuit
Size: A
Number:
Revision: B
File: VSWR0000.SCH
Date: 21-May-1997 Time: 16:06:19
Sheet 2 of 3
ERIM
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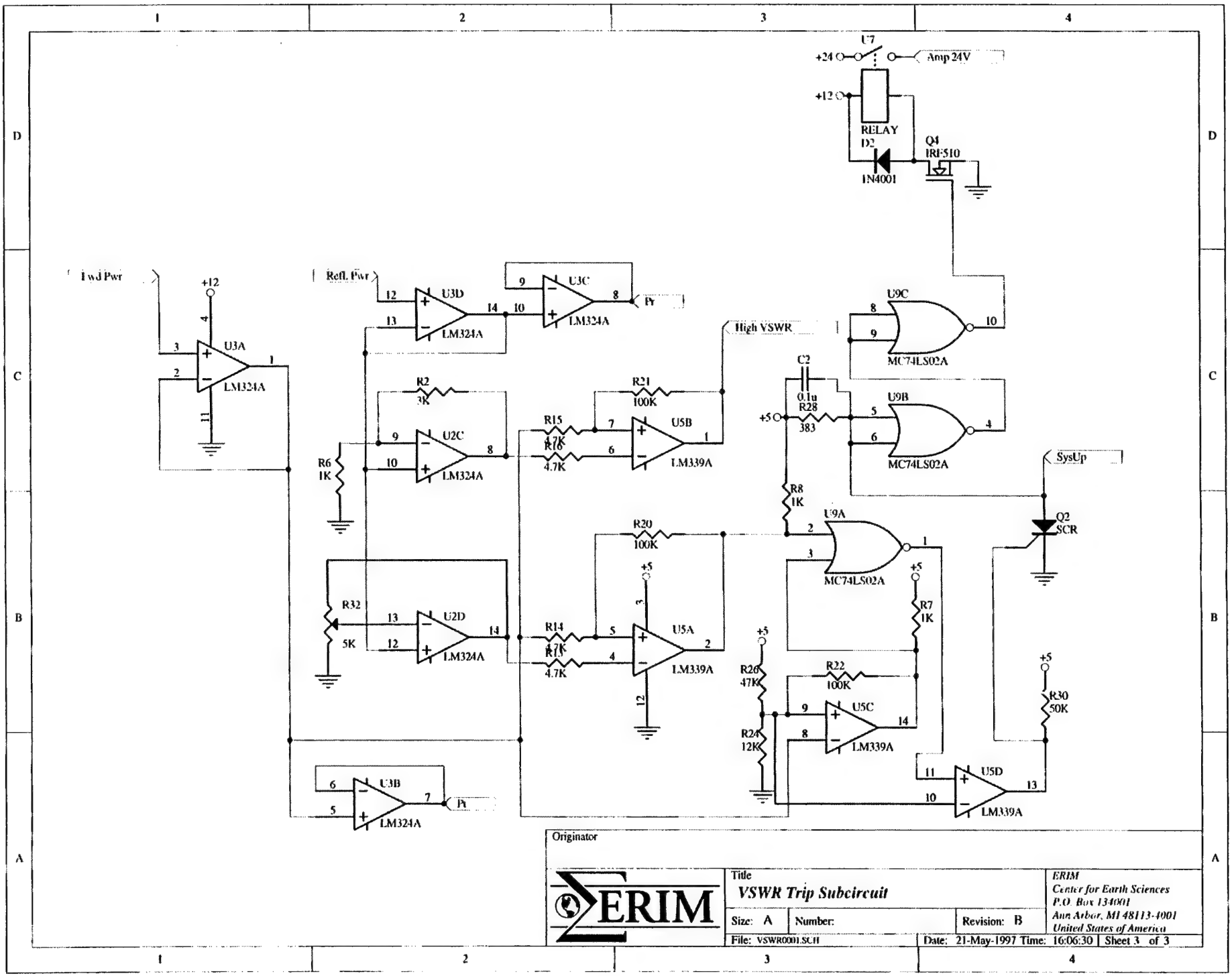
United States of America


U7
+24
Amp 24V
+12
RELAY
D2
1N4001
Q4
IRF510
Fwd Pwr
Refl. Pwr
+12
U3A
LM324A
U3D
U3C
Pf
High VSWR
U9C
MC74LS02A
C2
0.1u
R28
383
U9B
MC74LS02A
SysUp
R2
3K
R21
100K
R15
4.7K
R16
4.7K
U5B
LM339A
U2C
LM324A
R6
1K
R8
1K
U9A
MC74LS02A
Q2
SCR
R20
100K
R32
5K
U2D
LM324A
R14
4.7K
R17
4.7K
U5A
LM339A
R7
1K
R26
47K
R22
100K
R30
50K
U5C
LM339A
R24
12K
U5D
LM339A
U3B
LM324A
Pi
Originator
ERIM
Title
VSWR Trip Subcircuit
Size: A
Number:
Revision: B
File: VSWR0001.SCH
Date: 21-May-1997 Time: 16:06:30
Sheet 3 of 3
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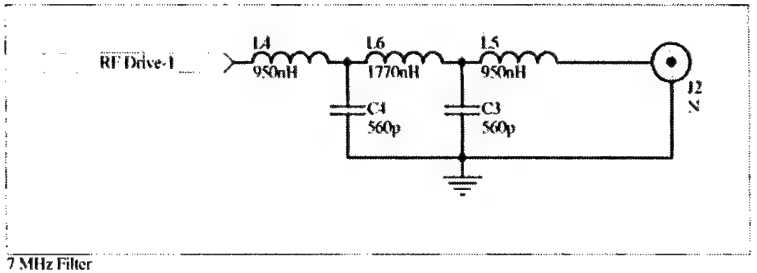
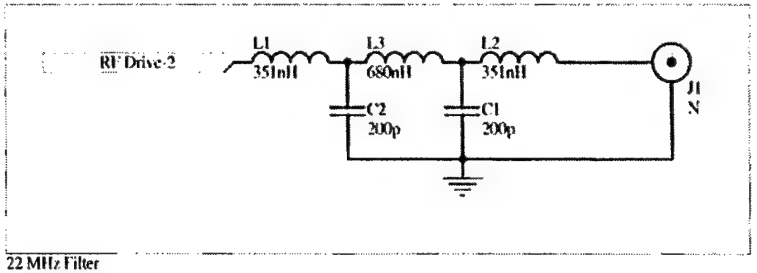


7 MHz Filter



22 MHz Filter

Originator

ERIM

Title
HF-Radar Low-Pass Filters

Size: A | Number: | Revision: A

File: DAPROJECTS\HFRADAR\LOWPASS.SCH | Date: 21-May-1997 Time: 16:01:39 | Sheet 1 of 1

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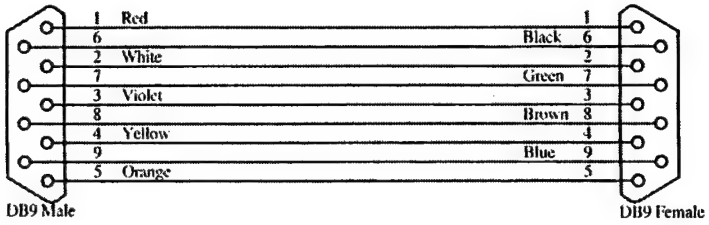
Pin	Voltage
1	+12
2	+5
3	5V/12V Rtn
4	5V/12V Rtn
5	-5
6	-12
7	NC
8	+24
9	+24 Rtn



Note: Cables are 3 feet in length

Originator

ERIM

Title
Power Interconnection Cables

Size: A | Number: | Revision: A

File: D:\PROJECTS\HFRADAR\POWERCBL.SCH Date: 21-May-1997 Time: 16:03:27 | Sheet 1 of 1

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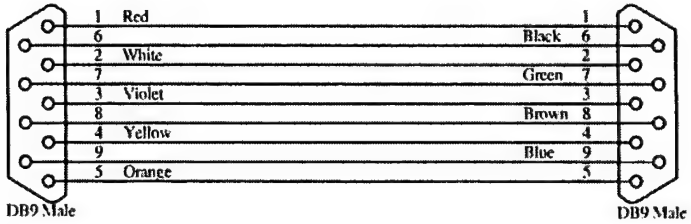

Note: Cables are 3 feet in length

Originator

ERIM

Title
Data Interconnection Cables

Size: A | Number: | Revision: A

File: D:\PROJECTS\HFRADAR\DATACBL.SCH | Date: 21-May-1997 Time: 16:02:17 | Sheet 1 of 1

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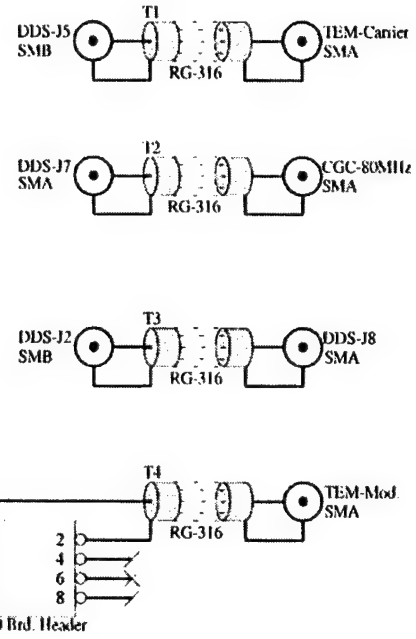

Originator

ERIM

Title
DDS RF Interface Cables

Size: A	Number:	Revision: A

File: D:\PROJECTS\HFRADAR\DDSCBLS.SCH Date: 21-May-1997 Time: 16:02:48 Sheet 1 of 1

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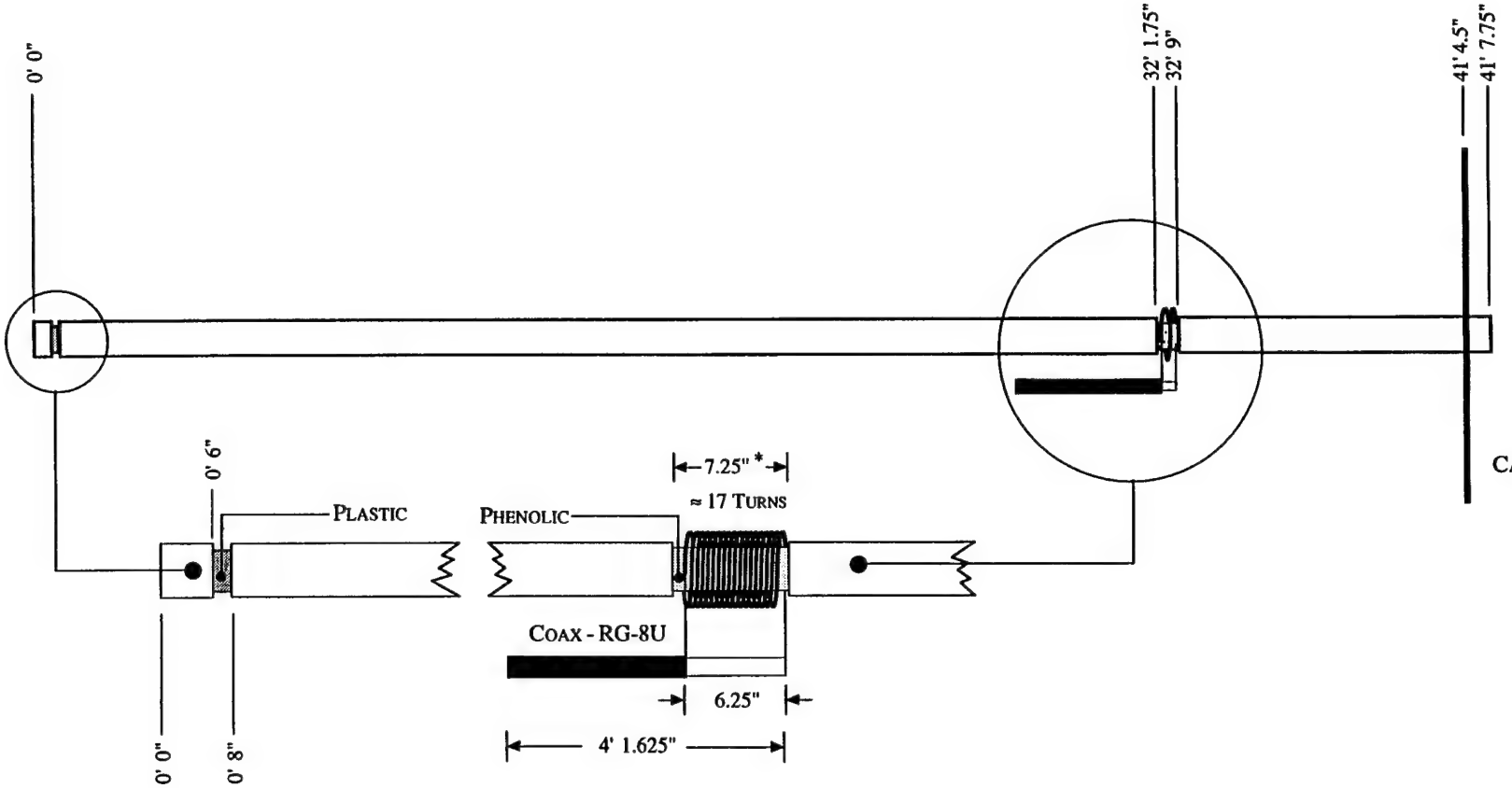
Vertical Monopole Antenna Assembly

Low Band Antenna (4.80 & 6.78 MHz)

1- Assembles using stainless steel clamps and inserts.
2- See diagram for length set points.
3- Trap inserts with RG-8 cable pointed toward ground
4- Trap conducting lines fit under cable clamps to make conduction.
5- Cable guide with three point mounting is included. The mount is placed immediately below the trap (See photo)
6- Capacitance hat fits at the top of the very top of antenna. The Capacitance hat is formed from two rod assemblies which are mounted orthogonally from each other.
7- Sixteen gauge wire is provided for the radials. Four ¼ wavelength radials are used for each band. Radials are placed every 90 degrees about the ground plate. Two sets of radials is accommodated on the ground plate. Radials connect to the ground plate using 10-32 screws. The ends of the radials are positioned using spikes (not provided - pick up on-site).
8- Radial lengths are 51 feet 3.2 inches, and 36 feet and 2.25 inches.

High Band Antenna (13.38 & 21.77 MHz)

1- Assembles using stainless steel clamps and inserts.
2- See diagram for length set points.
3- Trap inserts with RG-8 cable pointed toward sky
4- Trap conducting lines fit under cable clamps to make conduction.
5- Cable guide with three point mounting is included. The mount is placed immediately below the trap (See photo)
6- Sixteen gauge wire is provided for the radials. Four ¼ wavelength radials are used for each band. Radials are placed every 90 degrees about the ground plate. Two sets of radials is accommodated on the ground plate. Radials connect to the ground plate using 10-32 screws. The ends of the radials are positioned using spikes (not provided - pick up on-site).
7- Radial lengths are 18 feet 1.125 inches, and 11 feet and 3.45 inches.



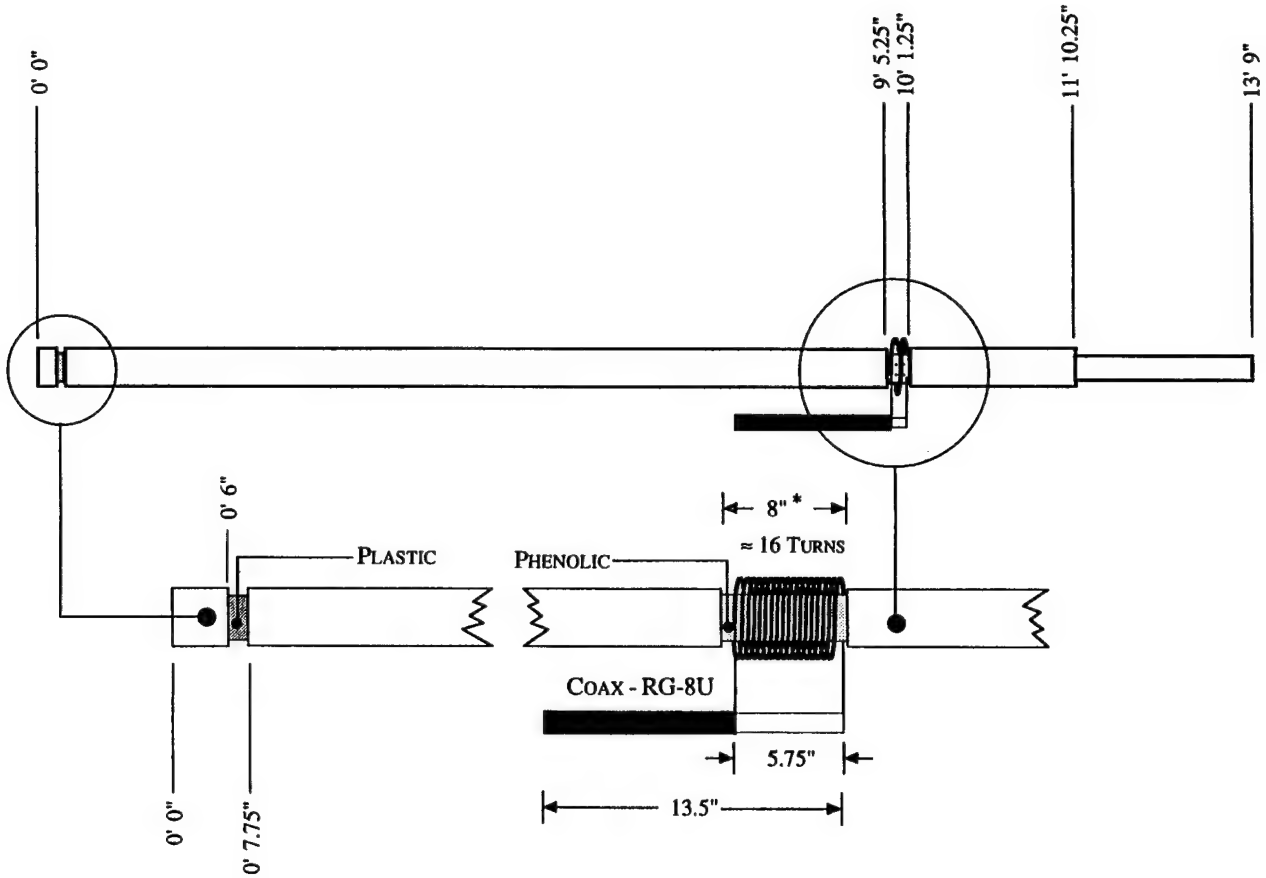
LOW BAND ANTENNA (4.80 & 6.78 MHz)

NOTES:

1. All sections of the antenna are aluminum except where noted.
2. All measurements were taken directly from the SN1 antenna as deployed at Santa Cruz 1/24/97 except where noted by an asterisk (*).
3. Heights of objects in drawing have been exaggerated to enhance legibility.

Space Physics Research Laboratory College of Engineering University of Michigan		Antenna Dimensions	REV REV REV RELEASE DRAWN COG ENG	 05-21-97 NS
PROJECT N000149510249	FILE NAME Ant Dimensions	DRAWING NUMBER 062- 0085	SHEET 3 OF 4	REV

Drawing Page



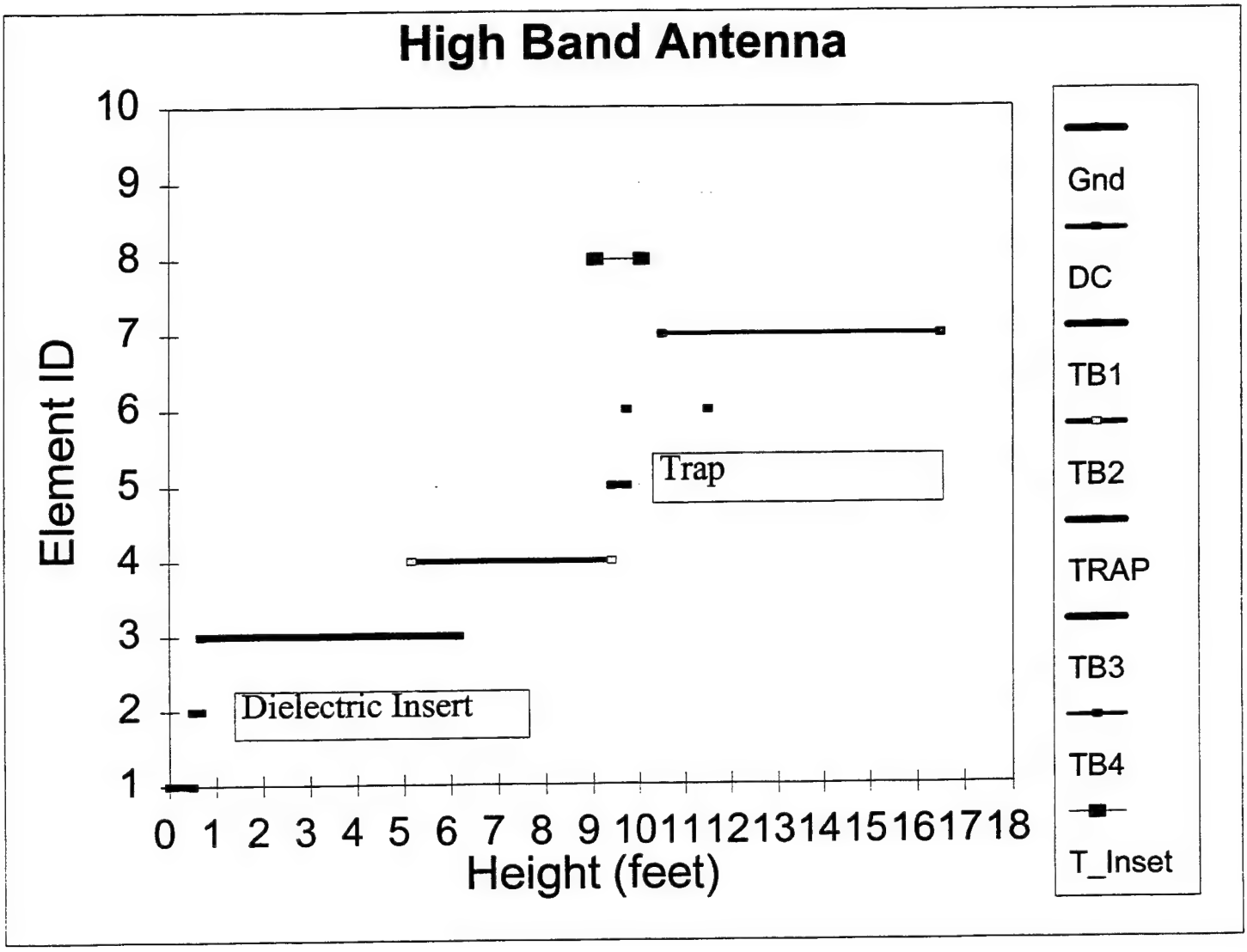
HIGH BAND ANTENNA (13.38 & 21.77 MHz)

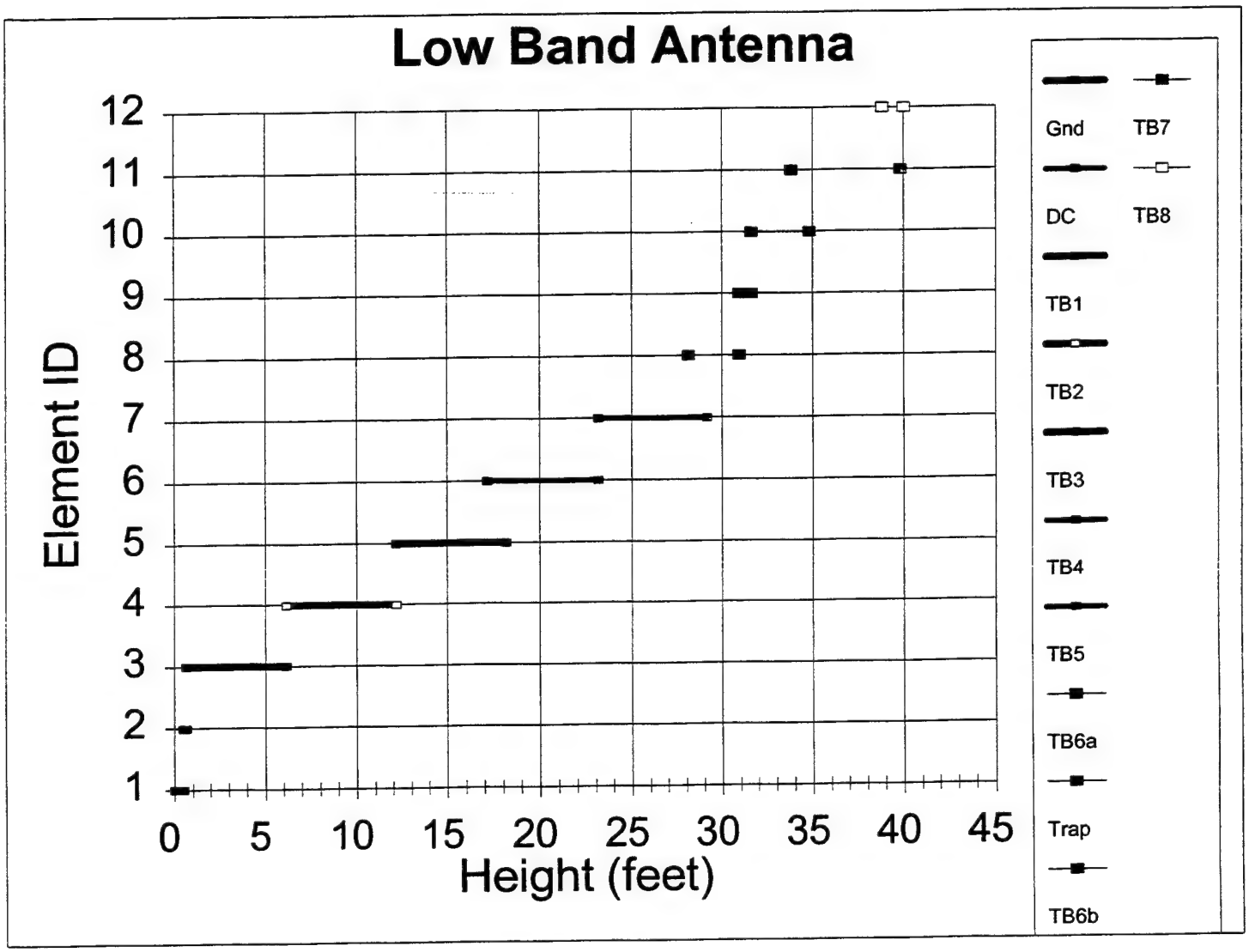
NOTES:

1. All sections of the antenna are aluminum except where noted.
2. All measurements were taken directly from the SN1 antenna as deployed at Santa Cruz 1/24/97 except where noted by an asterisk (*).
3. Heights of objects in drawing have been exaggerated to enhance legibility.

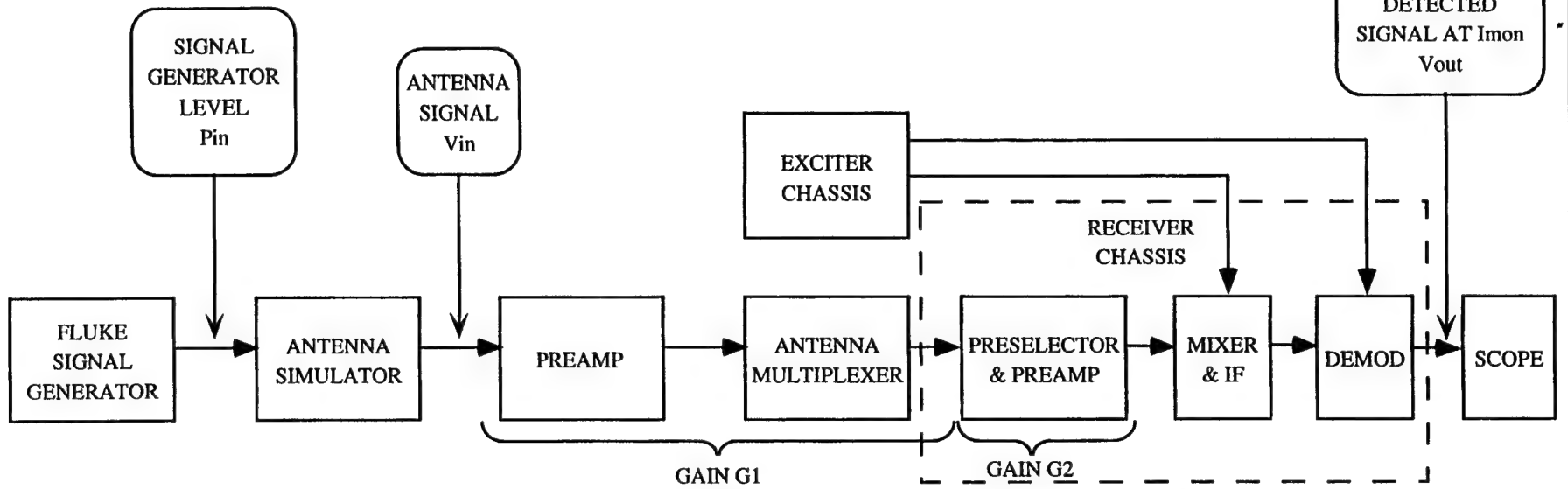
Space Physics Research Laboratory College of Engineering University of Michigan		Antenna Dimensions		REV REV REV RELEASE DRAWN COG ENG	 05-21-97 NS
PROJECT N000149510249	RELEASE Ant Dimensions	DRAWING NUMBER 062- 0085	SHEET 4 OF 4	REV x2	

Drawing Page


High Band Antenna
Element ID
10
9
8
7
6
5
4
3
2
1
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
Height (feet)
Trap
Dielectric Insert
Gnd
DC
TB1
TB2
TRAP
TB3
TB4
T_Inset


Low Band Antenna
Element ID
12
11
10
9
8
7
6
5
4
3
2
1
0
5
10
15
20
25
30
35
40
45
Height (feet)
Gnd
TB7
DC
TB8
TB1
TB2
TB3
TB4
TB5
TB6a
Trap
TB6b

SYSTEM PERFORMANCE DATA



GAIN G1 INCLUDES ALL CABLE LOSSES

SN 1 DATA

(TAKEN 20 SEPT 1996)

TYPICAL SIGNAL LEVELS			
Pin dBm	Vin uV	Receiver Gain Code	Vout Volts P-P
-80	1	1000	10
-70	3	900	11
-60	10	800	13
-50	30	700	6

NOTE: MINIMUM RECEIVER GAIN = 700, MAXIMUM USABLE RECEIVER GAIN = 1000

SN 2 DATA

(TAKEN 9 MAY 1997)

TYPICAL SIGNAL LEVELS

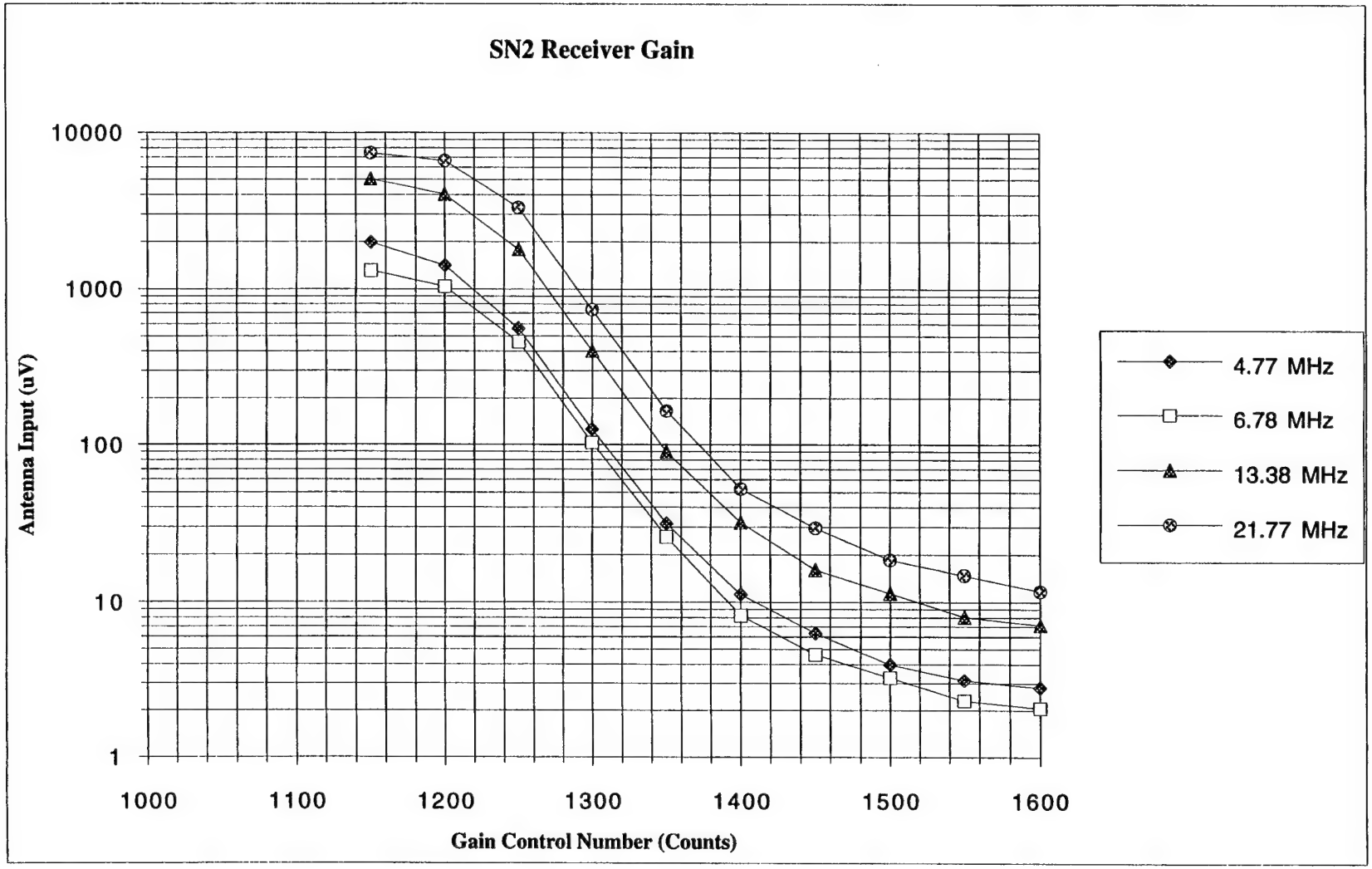
Pin dBm	Vin uV	Receiver Gain Code	Vout Volts P-P
-77	1.66	1600	10

NOTE: MINIMUM RECEIVER GAIN = 1100, MAXIMUM USABLE RECEIVER GAIN = 1600

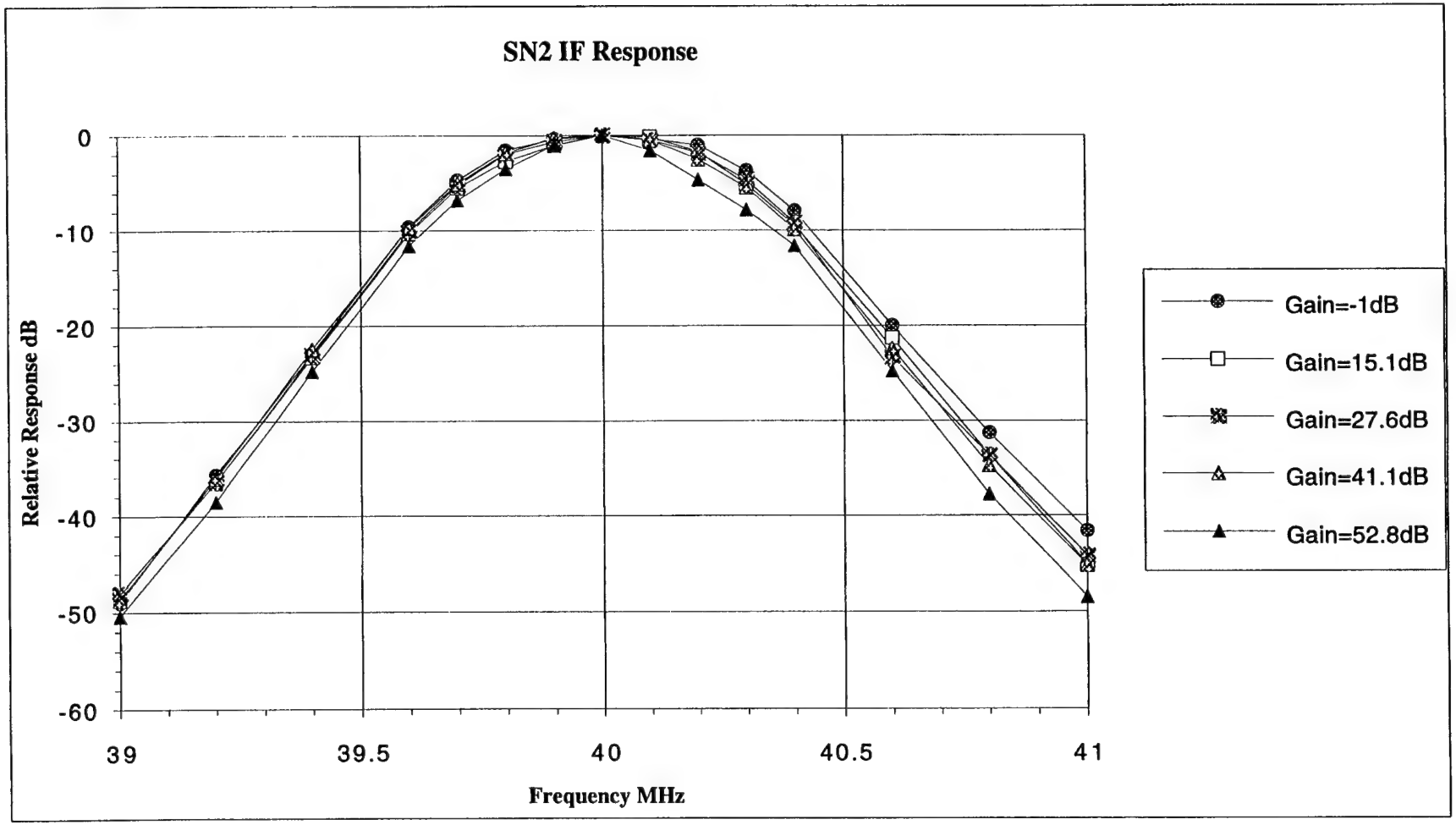
FREQ MHZ	GAIN G1 DB	GAIN G2 DB	G1 + G2 DB
4.77	17.2	16.8	34
6.78	17.9	17.8	35.7
13.38	11.7	14.2	25.9
21.77	8.3	15.3	23.6

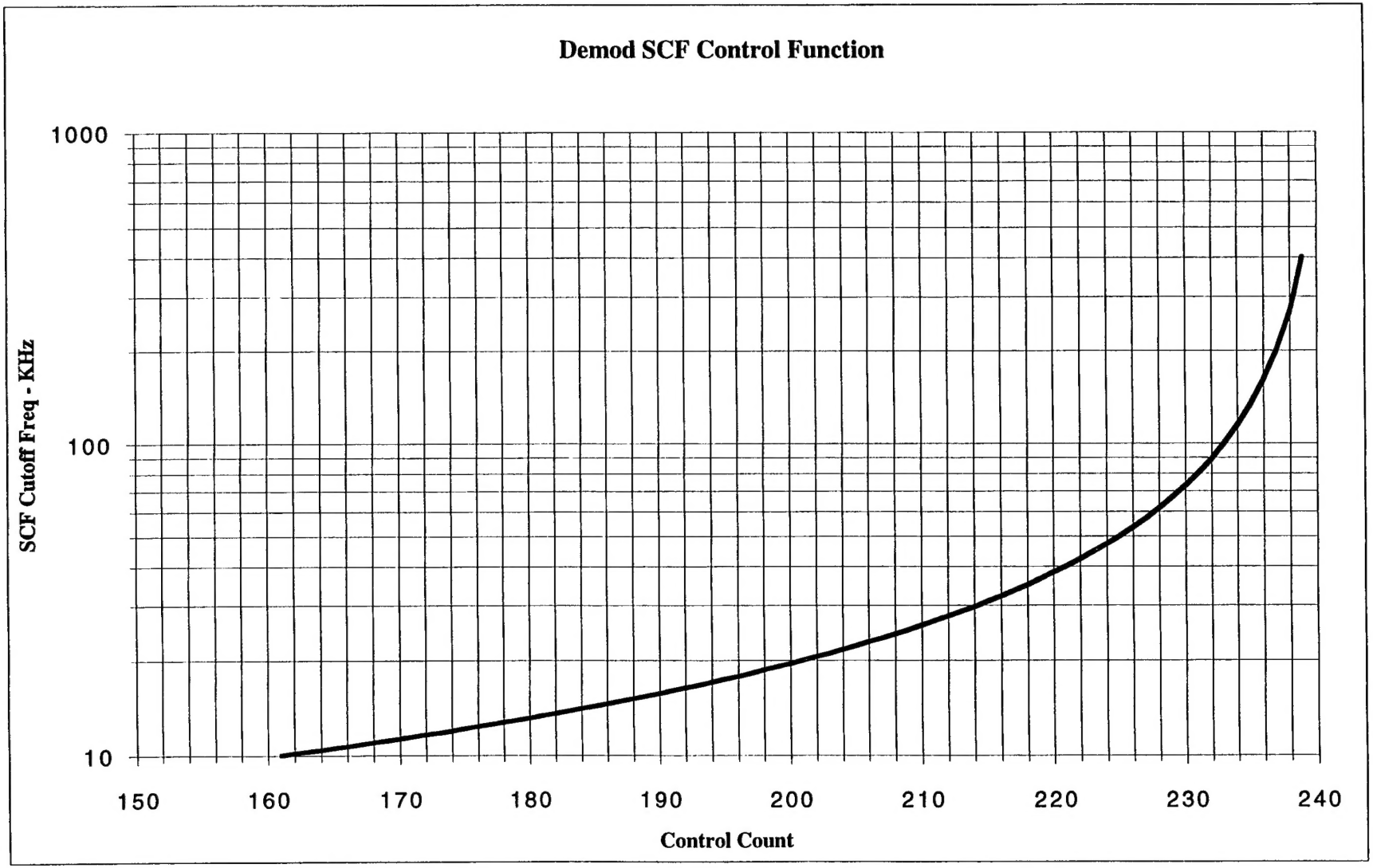
Space Physics Research Laboratory College of Engineering University of Michigan		RECEIVER TRANSFER FCN	REV REV REV 05-01-97 NS RELEASE DRAWN COG ENG
PROJECT N000149510249	FILE NAME Rcvr Xfer Function	DRAWING NUMBER 062- 0160	SHEET 1 OF 1 REV X1

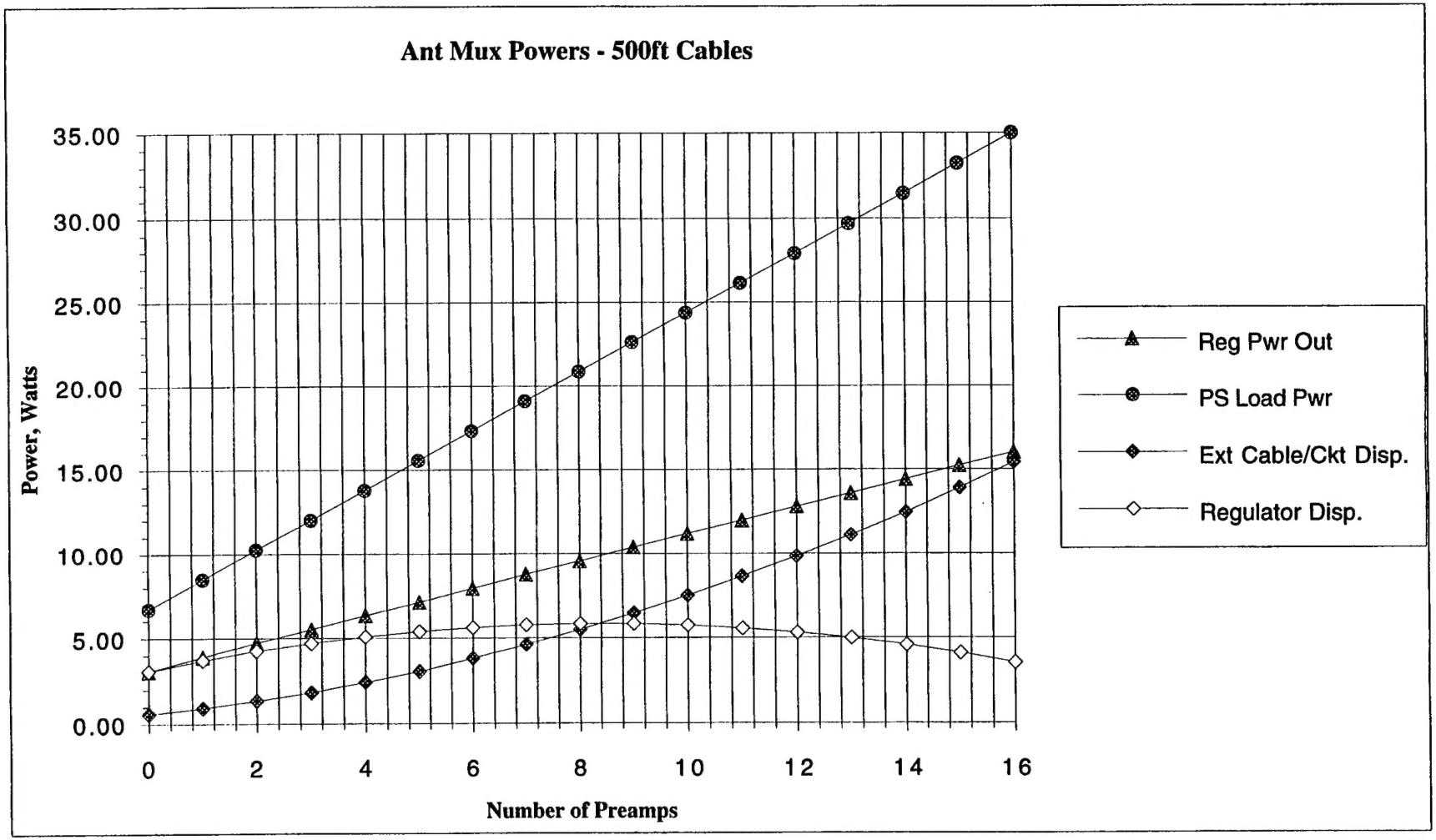
Drawing Page

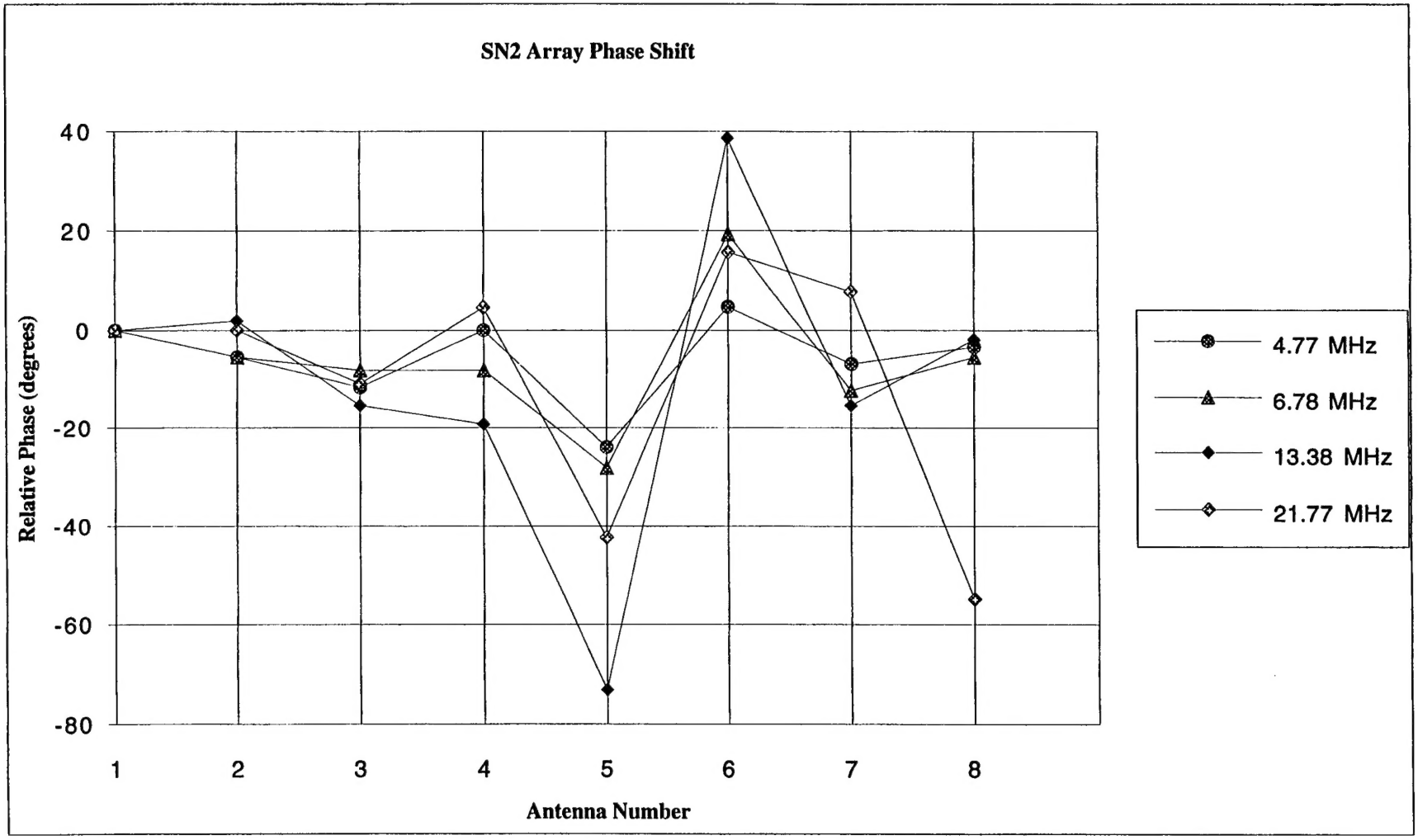

SN2 Receiver Gain
10000
1000
100
10
1
Antenna Input (uV)
1000
1100
1200
1300
1400
1500
1600
Gain Control Number (Counts)
4.77 MHz
6.78 MHz
13.38 MHz
21.77 MHz

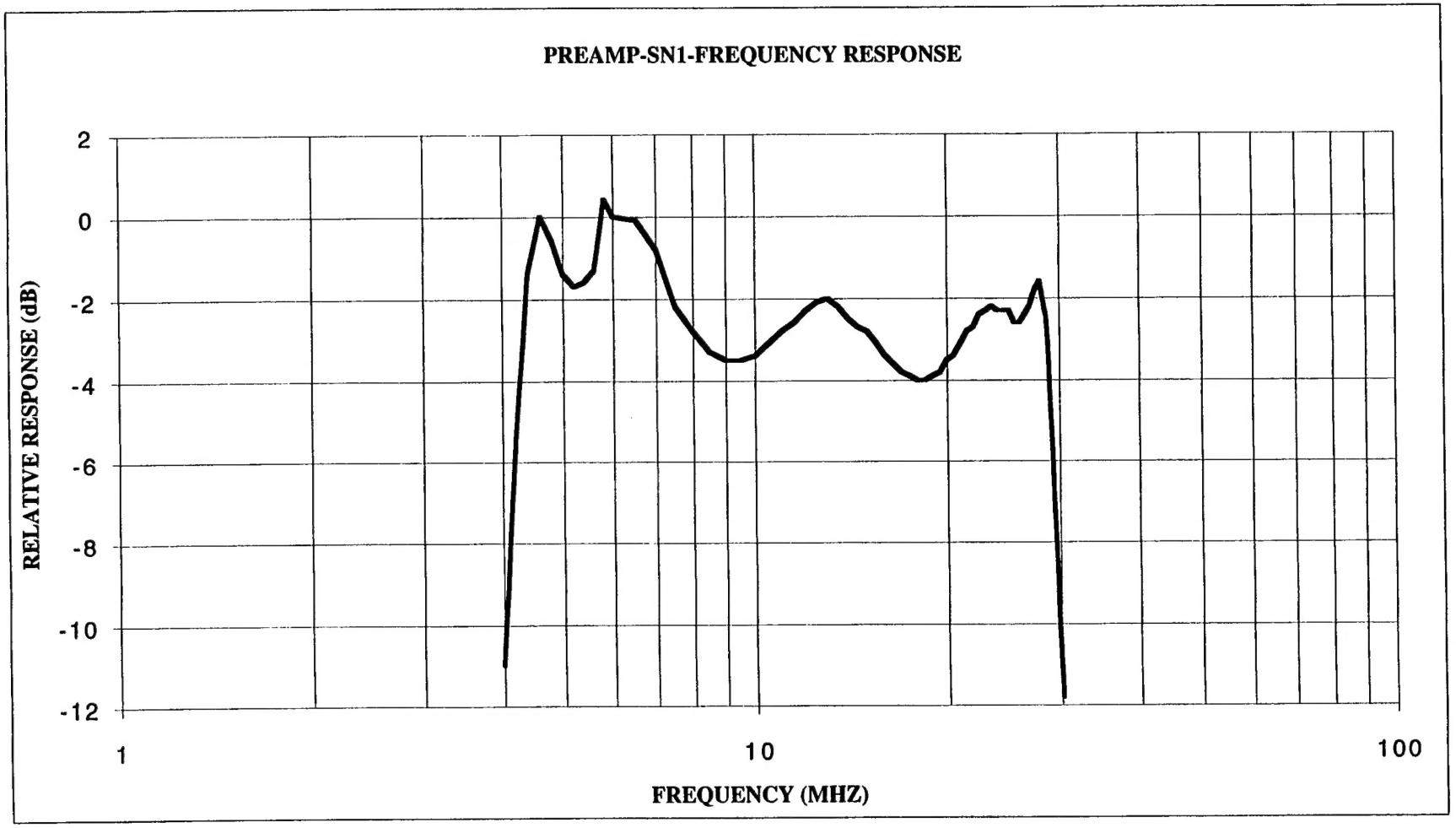
SN2 Gain Calibration Data												
Taken 1 May 97			Front End Avg Gain									
Signal levels in chart			Ant Terminals to Mix/IF J1									
are for 10 v p-p output from			dB	MHz								
demod/A-D interface			34	4.77								
			35.7	6.78								
			25.9	13.38								
			23.6	21.77								
Gain	4.77	4.77	4.77	6.78	6.78	6.78	13.38	13.38	13.38	21.77	21.77	21.77
Code	J1 Sig	Ant Sig	Ant Sig	J1 Sig	Ant Sig	Ant Sig	J1 Sig	Ant Sig	Ant Sig	J1 Sig	Ant Sig	Ant Sig
	dBm	dBm	uV	dBm	dBm	uV	dBm	dBm	uV	dBm	dBm	uV
1150	-7	-41	1992.9	-9	-44.7	1301.6	-7	-32.9	5063.9	-6	-29.6	7404.3
1200	-10	-44	1410.9	-11	-46.7	1033.9	-9	-34.9	4022.4	-7	-30.6	6599.1
1250	-18	-52	561.7	-18	-53.7	461.8	-16	-41.9	1796.7	-13	-36.6	3307.4
1300	-31	-65	125.7	-31	-66.7	103.4	-29	-54.9	402.2	-26	-49.6	740.4
1350	-43	-77	31.6	-43	-78.7	26.0	-42	-67.9	90.1	-39	-62.6	165.8
1400	-52	-86	11.2	-53	-88.7	8.2	-51	-76.9	32.0	-49	-72.6	52.4
1450	-57	-91	6.3	-58	-93.7	4.6	-57	-82.9	16.0	-54	-77.6	29.5
1500	-61	-95	4.0	-61	-96.7	3.3	-60	-85.9	11.3	-58	-81.6	18.6
1550	-63	-97	3.2	-64	-99.7	2.3	-63	-88.9	8.0	-60	-83.6	14.8
1600	-64	-98	2.8	-65	-100.7	2.1	-64	-89.9	7.2	-62	-85.6	11.7


SN2 IF Response
0
-10
-20
-30
-40
-50
-60
Relative Response dB
39
39.5
40
40.5
41
Frequency MHz
Gain=-1dB
Gain=15.1dB
Gain=27.6dB
Gain=41.1dB
Gain=52.8dB


Demod SCF Control Function
1000
100
10
SCF Cutoff Freq - KHz
150
160
170
180
190
200
210
220
230
240
Control Count


Ant Mux Powers - 500ft Cables
35.00
30.00
25.00
20.00
15.00
10.00
5.00
0.00
Power, Watts
0
2
4
6
8
10
12
14
16
Number of Preamps
Reg Pwr Out
PS Load Pwr
Ext Cable/Ckt Disp.
Regulator Disp.


SN2 Array Phase Shift
Relative Phase (degrees)
40
20
0
-20
-40
-60
-80
1
2
3
4
5
6
7
8
Antenna Number
4.77 MHz
6.78 MHz
13.38 MHz
21.77 MHz


PREAMP-SN1-FREQUENCY RESPONSE
RELATIVE RESPONSE (dB)
2
0
-2
-4
-6
-8
-10
-12
1
10
100
FREQUENCY (MHZ)